DFS Initial Design Guide

This document is to guide you through the process of designing your specific DFS implementation – it will help you determine the frequency mix, divider ratios, and filters required for your output frequency.

Note that there is also other documentation on the DFS website specifically aimed at helping you through this process – there is an Excel Frequency Calculation worksheet and a Configuration Document, as well as comprehensive lists of possible LO replacement schemas for DEMI and DB6NT transverters. You should consult these in addition to this document.

For variants that have been built and proven, there are version specific notes to be found on the website, giving a lot of detail about that implementation. This information is being expanded as new versions are completed.

Will it work?

Probably the most difficult part is finding a frequency mix that will produce your wanted output frequency. The table below gives the options for the most popular transverter LO's , based on a 144MHz IF up to 24GHz. Note that these can all be achieved using a 10MHz reference input frequency.

Band	Alloc	LO	Mult	Fundamental	Main	Loop 1	Loop 2
902	US	758	8	94.75	90	4	0.75
1296	All	1152	12	96	90	6	
2304	US	2160	24	90	90		
2320	EU	2176	24	90.6667	90		0.6667
2424	JA	2280	24	95	90	5	
3400	UK	3256	32	101.75	110	8	0.25
3456	US	3312	36	92	90	2	
5760	All	5616	54	104	110	6	
10368*	All	10224	108	94.6667	90	4	0.6667
24048	All	23904	216	110.6667	110		0.6667

* Information shown is for DEMI 10GHz transverter

Table 1 – Derivation of popular transverter LO frequencies from 10MHz ref input

Additionally, some frequencies can also be generated from a 15MHz reference input, as shown in Table 2:

Band	Alloc	LO	Mult	Fundamental	Main	Loop 1	Loop 2
1296	All	1152	12	96	105	9	
2304	US	2160	24	90	90		
2424	JA	2280	24	95	105	10	
5760	All	5616	54	104	105	1	

10368*	All	10224	108	106.5	105	1.5	

* Information shown is for DB6NT 10GHz transverter

Table 2 – Derivation of LO frequencies from 15MHz ref input

Note that the majority of these solutions are single loop implementations – only 3 require the full two loop deisgn. You will also see that for some bands there is more than one way to assemble the frequency you need – in such cases you should consider the starting frequency you have available – 10 or 15MHz, and also the filtering of the mixing products that wll be generated. For example, for a 10GHz DB6NT transverter, requiring a 106.5MHz LO input, there are two solutions possible from a 10MHz input – 90+15+1.5MHz and 110-(3+0.5)MHz – of these the first solution based on 90MHz should give the easier filtering needs. However, these are both 2 loop solutions. By using 15MHz as the ref frequency, the design is simplified to 105 +1.5MHz – filtering is a little more demanding than the 90MHz route, but less products wil be generated, since one mixing process has been eliminated.

If you do need to generate a frequency mix that has not already been identified in the schema's referenced above, then do try to avoid solutions which have a very low frequency component as part of the set – the closer any mixing products are to your wanted frequency, the more difficult they will be to filter out, of course.

Further Options

Remember that in addition to simply feeding the second divider from the input, the first divider output, or its multiplied output, there are other (more complex) choices which may also solve your needs. For example, you could multiply the 10Mhz signal up to say 20, 30MHz etc, and use a divided portion of that. You could also take the 90MHz main signal directly and divide it – the dividers used will work in excess of 120MHz.

Note that the current PCB does not directly support these implementations - such connections would need to be carried out by 'cut and strap' techniques. All stages and filters are nominal 50R iput and output impedance, so apart from level differences, you should be able to connect things in a different order to the default PC layout.

As a final option, there is also a facility to add an external input. This could be used to bring in a low frequency signal from, for example, a DDS clocked by the GPS reference – provided the clock freq is kept much higher than the output frequency, the levels of spurii in the DDS output should not cause any significant degradation of the DFS performance. This option would allow you to mix almost any frequency with the multiplied and divided DFS signal, and therefore produce any required output frequency.

Remember however, that this will still not make it a tunable synthesiser, since the crystal filter in the out will only pass a very narrow band without signifiant added attenuation.

What next?

Having identified your component frequencies , you will also have determined which mixing product you need at each stage – the sum or the difference, so you can specify the filters needed at each stage. Data on filter solutions already proven are given on the Filters page of the DFS website.

The filter implementations available on the PCB are simple two pole low pass or band pass. If you prefer more complex filtering, then it is recommended that you create a small daughter board to replace that section on the PCB.

In both divider paths the PCB gives you the option to use an amplifier/multiplier or a straight low pass filter. If you do not need to multiply the frequency from the divider, then use the LPF – signal level is not an issue when you have a 5v switching signal from the logic!

Wherever possible, flexibility of implementation has been provided. For all of the variable inductors, you can use Toko S18, MC117 or MC120 styles, with or without cans, or the Coilcraft Unicoil 10 range. In order to reduce the possibility of unwanted sgnal paths, I recommend that you use the shielded coils if possible, or provide extra shielding between stages – the Iss 1 PCB has land available on the top side for attaching these shields.

For the lower frequency stages, transformers are used, which need to be fabricated from re-wound Toko 10K series coils – see my guidance on Rewinding Toko 10K Coils for advice on doing this.

I recommend that once you have designed each filter that you synthesise it in a suitable program – I use Ansoft Designer SV, the freeware student version – to confirm its performance.

A note on VHF Overtone crystal filters is warranted here – while using fundamental crystals to produce a filter is well understood, the use of crystals in their overtone modes in the VHF region is not! Try 'Googling' for VHF ladder filters, or similar, and see how many relevant hits you get!

The component values given here for the L's and C's in the crystal filter are empirical – they are known to work over a range of at least 90 to 125MHz. And if you're looking for a PhD thesis topic.....

The latest filter information is posted on the DFS website at http://g4hup.com/dfs/DFSdoc.html

The PCB

The G4HUP DFS PCB is intended as a 'breadboard'. It is there for experimentation, since there is such a tremendous variety of options and output frequency possibilities for DFS solutions! It has been designed so that what are probably the most common options are easy to select from the board, but that should not preclude its use in more complex or novel solutions – see GM8BJF's 92.25MHz DFS, as an example.

Circuit Stages

This design is meant to be flexible – so you only build what you actually need. For example, if you are not bothered about having a replicated 10MHz output, then ignore the splitter and attenuator on the output of the first stage. And if you already have around +10dBm available as an input level, eg a Z3801A, – then ingore the first stage completely – strap the input straight into the diode multiplier.

Similarly, with the various amplifer/ LPF options, and of course many implementations will only require a single loop – so a divider, a mixer and a whole line of filtering is not needed.

In this way, even though the PCB may appear complex, the final implementation may be relatively simple.

Attenuators

There are several points in the design where provision is made for resistive attenuators so that levels can be set to avoid overdriving stages, and consequently producing unnecessary frequency products. Most of these are shown on the diagrams with default values for 3dB – and in most cases you will not need to change this.

The only significant difference is the input buffer stage – the input attenuator value should be set so that the diode multiplier stage is being fed with approx +10dBm. GPSDO sources that I have tried seem to give around +9 to +11dBm output, and 7dB seems to be a good centre value for this attenuator when the MAV-11 is used as the gain block here.

Divider Programming

This is probably the most daunting part of the process for many! Actually it is quite simple, but has a few steps in it.

1. First identify the division ratio you want
2. Subtract that number from 16 – the answer is the number you need to program into the divider
3. Convert the answer into binary, and read it DCBA – ie A is the LSB and D is the MSB of the binary data.
4. Each binary 1 means 'connect to +5v (via the pull-up)' and each 0 means 'connect to ground'

For example, let's say you need to divide by 6:

1. 16 – 6 =10
2. Decimal 10 in binary is 1010
3. The D and B pins of the IC must be connected to the pull-up resistors, and pins C and A must be grounded.

4 So for example, if this was for the first divider, then pins 6(D) and 4(B) must be connected to the pull-ups. Pins 5(C) and 3(A) must have the solder jumpers places across SJ3 and SJ1 respectively.

I recommend that you do use the pull-up resistors provided. The 74161/163 counters do in fact have weak pull-ups included internally, but the use of an external pull-up is strongly recopmmended to reduce noise on the input pins and the likelihood of false counting. Don't forget, jitter (noise) in the dividers makes a contribution to the phase noise of your final DFS.

Although the pads for the pull-ups are close to the ends of the SMD jumper block, you may need to use a short length of wire to link over the top of a grounded pin – as for pin 4 (B) in the example above.

Choosing the Mixers and other Components

The PCB is designed to accomodate the standard Minicircuits Level +7 type mixer, in the A01 to A06 package. There are minor differences in connection of the IF port between these styles, but all should be OK on the board.

The actual mixers you use will be a trade off between cost, frequency range and availability. Try to select mixers wich are not operating at the edge of their frequency range.

For the lower frequency, the SBL1-1+ is a good compromise between performance and cost – but it only goes down to 100kHz, so I would try to use a lower frequency mixer for mixes that had a component of less than about 250kHz.

The higher frequency is less of a problem – the SBL-1 is fine for probably all applications of the DFS, and is probably Minicircuits cheapest mixer in this type of package.

Logic choices

74F family is probably the fastest, but is getting more difficult to obtain. However, the 74ACT will work to similar speeds, and is CMOS – which means a trade off between better noise immunity, but higher noise contribution to the putput than the F logic. I would recommend that you use the F range if you can obtain them. Also make sure that you use the pull-up resistors on the programming inputs – this helps to reduce noise.

And finally.....

If you want to do something and you can't find any leads or information to support you – e-mail me! Contact me at g4hup@btinternet.com, or via the Contact me link on the home page.

73, Dave, G4HUP / ND8P