G4HUP

Direct Frequency Synthesiser

Technical Manual

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Contents

Unit Specifications

Model Ref

Serial No

Input Frequency	10	MHz
Input Level	+10	dBm
Output Frequency		MHz
Output Level		dBm
HF Multiplier		
MF Divider Ratio		
MF Multiplier		
LF Divider Ratio		
LF Multiplier	-	
Supply Voltage	10 – 15	V
Supply Current		mA @ 13vdc
Spurii	<-60	dBc - typical
Harmonic output	<-45	dBc – second harmonic - typical

Scope of Document

This document is intended to provide all necessary information to guide users in the installation and configuration of the G4HUP Flexible DFS in normal operation.

Ready built units are supplied to agreed customer specification, and should require no configuration for initial use.

This document is relevant for DFS units constructed on Iss 1_0 PCB's.

Note that for the purposes of information, the circuits in this document are based on the example of a 94.667MHz synthesizer, since this exercises most of the circuit functions. The specific blocks implemented for an individual design will be selected according to the frequency schema required, and as such attenuators and filter designs must be adjusted to suit. Reference data can be found on the DFS web-site, which contains details of all reported implementations – http://g4hup.com/DFS.html . The site also contains typical frequency schemas for popular transverter LO's.

Frequency multiplies used in this manual are based on the assumption of a 10MHz input reference frequency. These must be adjusted if alternative frequencies are used – eg 15MHz.

DFS Description

The DFS is constructed in a tin-plate housing, measuring 148 x 74 x 30 mm (5.75 x 2.8 x 1.2 inches approx)

External connections are provided for:

- Reference signal in
- Buffered Reference signal out
- Output signal
- Optional External RF input
- +Vcc power supply
- 0v DC ground

All RF connections use SMA female panel connectors

DC connections are by solder terminations to the DC input feedthrough capacitor and the ground tag close by it.

The main circuit blocks are shown in Fig 1, and are described in the following sections, which refer to the circuit diagrams at the end of this manual.

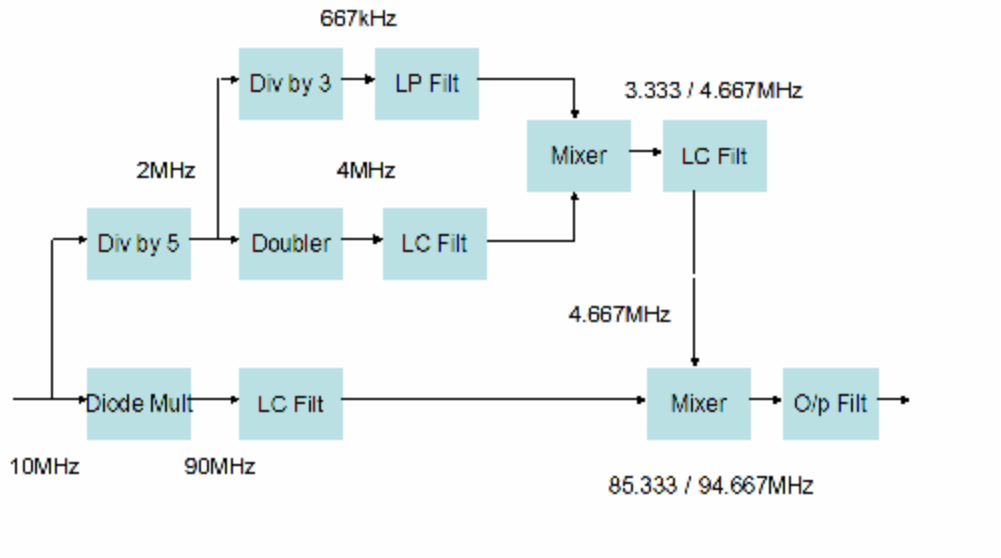

Fig 1 – DFS block functions
NB – frequencies quoted are for indication only

Input Buffer Circuit – Fig 2

NB – this circuit block is not included in the Fig 1

The input buffer circuit comprises of an attenuator, MMIC buffer amplifier, resistive splitter and a second attenuator.

The input attenuator, Atten 1, should be set so that the output of the resistive splitter provides +10dBm drive into the diode multiplier stage. As supplied, the attenuator will be configured for 7dB, which is the correct value for a nominal +10dBm input, as provided by an HP Z3801A GPS Disciplined Oscillator source. For other reference frequency sources, adjustment of the attenuator value may be required to achieve the correct drive.

A value of 3dB is set nominally on the second attenuator, Atten 2,which feeds the buffered output socket – this also can be adjusted to suit any following use of the output signal. It is **not** necessary to terminate this output in 50R in the case where it is unused.

The drive to the multiplier and divider stages is via the resistive splitter.

When a drive source of +10dBm or greater is available, and no buffered output is required, this stage can be omitted. In this case strap the input connector directly through to the point where the diode multiplier and the coupling into the logic dividers connect together (junction of C401, L021 and L202). The attenuator stage can be implemented if the drive level is significantly above +10dBm.

Diode Multiplier – Fig 3

The diode multiplier is a comb generator, and produces output components beyond 400MHz. The following filter selects the 90MHz component and reduces the levels of the others to insignificant levels.

This filter, F1, is a two stage LC filter, using inductive coupling. Capacitive taps are used at input and output to match into the surrounding stages.

Two stages of MMIC amplifier are use to bring the 90MHz to a suitable level to drive the double balanced mixer that follows. Atten 3 can be used to adjust the drive level into the mixer. If it is not required then R204 should be replaced with a short circuit, and R203 and 205 omitted. This principle applies to all other attenuators in the circuit.

Logic Stage – Fig 4

The logic stages use fast logic – 74F or 74ACT series – to ensure optimum performance – these devices are capable of counting to frequencies in excess of 120MHz.

The input signal is taken from the Input Buffer via C401. IC401/6 buffers the signal and produces a logic level square wave – the input to this gate is biased by R401 and R402 to make sure the input signal is in the correct range for a good switching action.

Both divider IC's have programmable inputs using SMD solder links SJ-14 and SJ9-12. the 'wanted' combination of program inputs should be solder linked across to ground, and any remaining open inputs connected to the pull-up resistors R403 – R406. This reduces noise on the unused inputs, and improves the jitter performance of the logic stages.

The output from each divider is also selectable on links SJ5-8 and SJ13-16. For direct outputs, or where an odd harmonic multiplication is to be used, choose the output with the closest to a square wave output – often pin 13. For even harmonic multipliers, an output duty ratio of 80/20 is better.

Each IC has optional LC decoupling on the supply to reduce the switching transients that may be fed back to analogue parts of the circuit. If you choose not to use this, replace each L by a short circuit, and omit the capacitor physically furthest away from the power pin of the IC.

MF Multiplier – Fig 5

The amplifier/multiplier or low pass filter are selected via SJ901 and SJ902. In this model the multiplier is used.

A single transistor amplifier stage, TR901, has the tank circuit in the collector tuned to a harmonic – this is link coupled to a second tuned circuit. These two tuned circuits constitute the filter F2.

Alternatively, the LPF, F3, can be used where the output frequency from the divider is the wanted one. It may also be usable for a x2 multiplication when the duty cycle of the divider output is 80/20.

Following SJ902 there is an attenuator, Atten 4, to adjust the level into the low frequency mixer.

LF Low Pass Filter – Fig 6

As with the MF stage, the LF stage has the option of either amplifier/multiplier, F4, or low pass filter, F5. In this case, only the low pass filter, F4, is required – selected by SJ301 and SJ302.

Again, there is an attenuator, Atten 5, following SJ302, to set the correct levels for the mixer.

An external SMA input, X301, is shown on this diagram – this may be used where an external signal is to be fed into the mix, such as that from a GPSDO controlled DDS, instead of taking an output from the second divider. If this is not required, ignore this option.

Low Frequency Mixer – Fig 7

The low frequency mixer combines the MF and LF signals, using an SBL1-1+ mixer, specified from 100kHz to 400MHz. This is followed by a single transistor amplifier and three poles of filtering – the tank circuit of the amplifier stage, and a two stage, top-coupled LC filter, F6. The IF output is approx 1350mV p-p – more than adequate to drive the high frequency mixer. Attenuator Atten 6 is used to reduce this by 3dB.

Alternative mixers may be used in this stage according to the frequencies used – check the specification on the Minicircuits website.

High Frequency Mixer – Fig 8

The second mixer combines the 90MHz signal from the multiplier chain with the 4.667MHz generated by the low frequency loop. It uses an SBL-1 mixer, and is followed by a two stage LC top-coupled filter, F7, to reduce the 85.333MHz and 90MHz components out of the mixer.

Alternative mixers that can be used here include the SRA-1, other SBL1 variants and many others – again, check the Minicircuits website for specifications.

An MAR-6 MMIC amplifier is used to bring up the signal level – this is followed by an attenuator, Atten 7, for gain adjustment

Crystal Filter and Output Amplifier – Fig 9

A 3 stage crystal filter, F8, using 5^{th} overtone crystals is used to reduce close-in products to the wanted frequency. Careful tuning is required to obtain the best symmetry and balance in the output spurii.

Another MAR6 MMIC forms the output amplifier, again with a following attenuator, Atten 8.

The final stage is a low pass filter, F9, to limit the harmonic content present in the output. This provides approx 21dB of suppression at the second harmonic and at least 48dB third harmonic and above.

Voltage Regulators – Fig 10

Two 1A IC voltage regulators provide the 5v and 8v rails – these use the metalwork of the tin-plate case for heat dispersion.

Filter and Attenuator Settings

The following tables identify the components associated with each attenuator and filter, and the specific settings implemented in the sample to which this manual refers.

Attenuators

Ident	Value	Comment	Implemented
Atten 1			
R1,2,3	130R, 43R, 130R	7dB input atten	yes
Atten 2			
R8,9,10	270R, 15R, 270R	3dB buffer output atten	yes
Atten 3		3dB atten – input to HF mixer	no
R203,204,205	270R, 15R, 270R		
Atten 4			
R903, 904, 905	270R, 15R, 270R	3dB mixer input atten	yes
Atten 4			
R303, 304, 305	270R, 15R, 270R	3dB mixer input atten	yes
Atten 5			
R504, 505, 506	270R, 15R, 270R	3dB mixer input atten	yes
Atten 6			
R602, 603, 604	270R, 15R, 270R	3dB gain adj atten	no
Atten 7			
R702, 703, 704	270R, 15R, 270R	3dB gain adj atten	no

Filters

Ident	Value	Comment	Implemented
F1			
C202, 203	220p, 18p	90MHz selection from 10MHz comb	yes
L205, 206	180nH		yes
C204	18p		yes
C205, 206	220p		yes
C206, L207			no
F2			
C904		4MHz selection filter	yes
T901, 902	2u8H		yes
C905			yes
F3		2MHz LPF	no
C906, 909			no
C907, 908			no
L901, 902, 903			no
F4			
C302	1n9	667kHz amplifier filter	no
T301	37uH		no
F5			
C305, 308	5n6	667kHz LPF	yes
C306, 307	10n		yes
L301, 302, 303	15uH		yes
F6			
C502	220p	4.667MHz post mixer filter	yes
C503			no
T501, 502, 503	6u8H		yes
C506, 507	3n3, 150p		yes
C508	10p		yes
C509, 510	150p, 3n3		yes
F7			
C601, 602	220p, 33p	94.667MHz post mixer filter	yes
L601, 602	100nH		yes
C603	0p4		yes
C604, 605	33p, 220p		yes
F8			

C701, 703, 705, 707	56p	94.6667MHz crystal filter	yes
L701, 703, 705, 707	56nH		yes
Q701, 702, 703	94.6667MHz 5OVT		yes
C702, 704, 706	20p trimmer		yes
L702, 704, 706	220nH		yes
F9			
C712, 714	22p	Output LPF – harmonic reduction	yes
C713	56p		yes
L708, 709	100nH		yes

See http://g4hup.com for full and latest information on filters.

Errata and Addenda

This section contains information about components that have been changed or added compared with the original PCB design.

1. R401 does not have a ground connection on Issue 1 PCB's – this must be provided by a short strap of wire to the ground side of L201.
2. There is no +5v Vcc connection to TR301 on Sheet3. 5v is present at the via through the PCB, but there is a short track missing between the via and the junction of R302 and C303. This can be bridged with a blob of solder.
3. There is a track error in the logic section – Sheet 2. Pins 5 and 10 of the hex inverter, IC401, are erroneously connected. This can be corrected by cut and strap.
4. Documentation error – the screen print legend on the PCB underside shows R11, 12 and 13, instead of R203, 204 and 205 at the output of the diode multiplier amplifier chain – Sheet 2

See http://g4hup.com/DFSerrata.html for full details, versions impacted and resolution guidance, including pictorial support.

Voltage Regulators – Fig 10

Not shown on the diagram is the 1nF feedthrough capacitor, C809, which is used to bring the nominal +12v DC into the circuit enclosure.

Component Locations

Figs 11 and 12 respectively show the locations of components on the top side and lower side of the PCB

Maintenance

Construction Practices

This unit has been assembled using lead bearing solder - any repairs or changes necessary should be made using lead based solder. Use as small a grade of good quality flux based electronic assembly solder as possible.

Change History

Date	Iss No	Comment	Author
16 Oct 2007	1.0	First version	G4HUP
3 Nov 2007	1.01	Errata on PCB Issue 1, Filter reference added	G4HUP
20 Nov 07	1.02	Errata in F1 implementation component ID's, Errata updated	G4HUP
5 Dec 2007	1.03	IC references in Fig 4 corrected, Errata updated	G4HUP

End of text – Diagrams follow

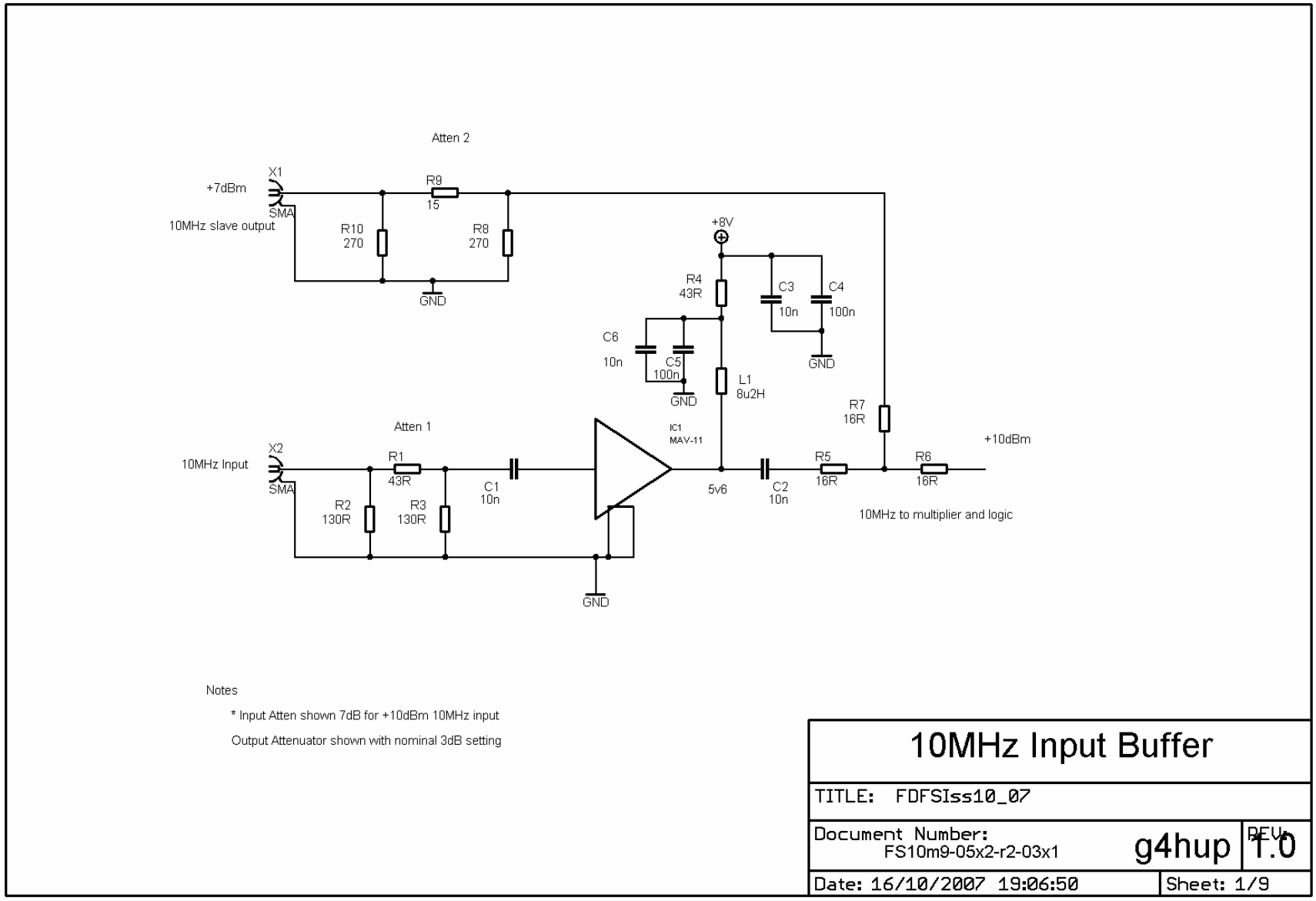

Fig 2 – Input Buffer Circuit Schematic

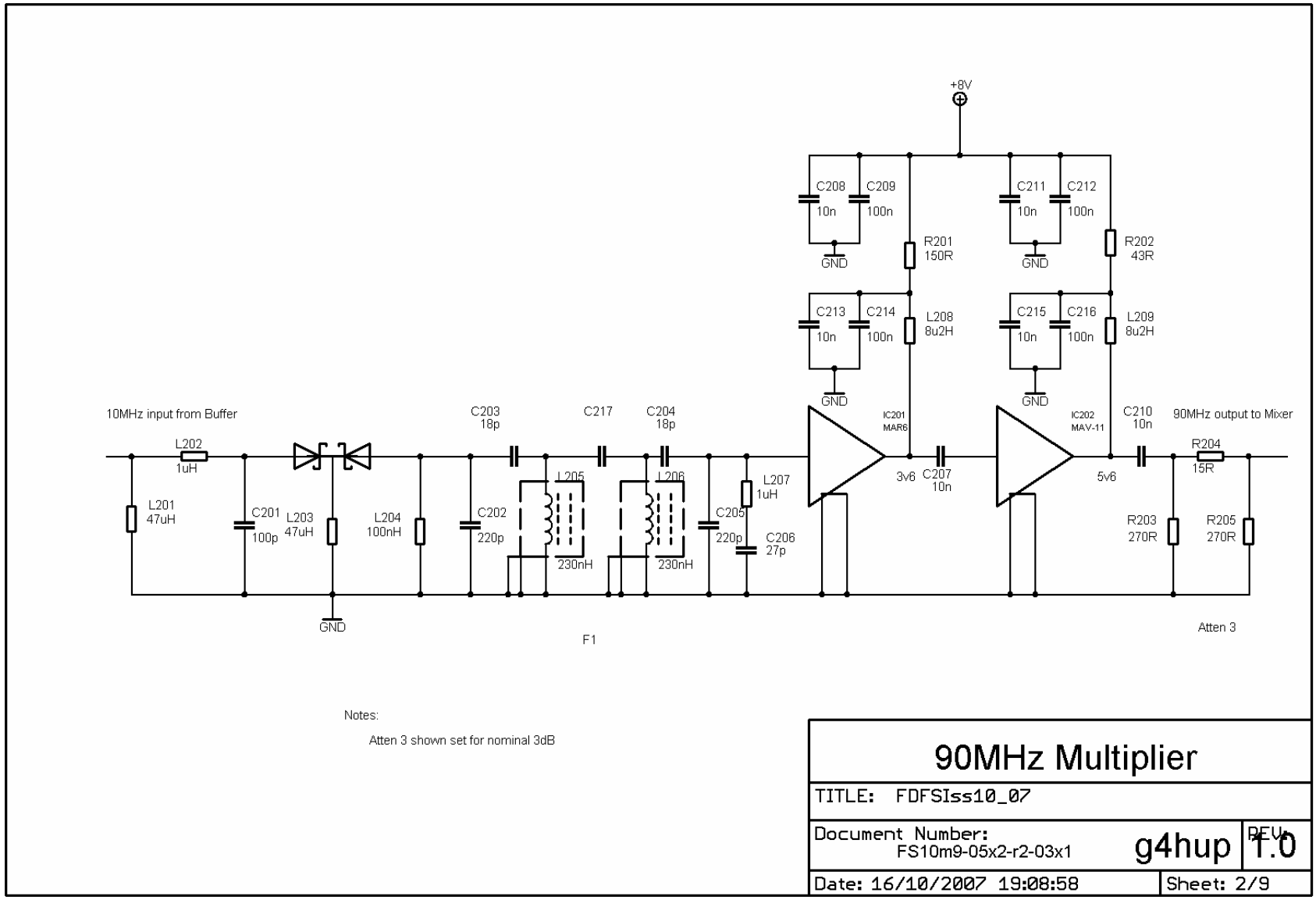

Fig 3 – Diode Multiplier Circuit Schematic

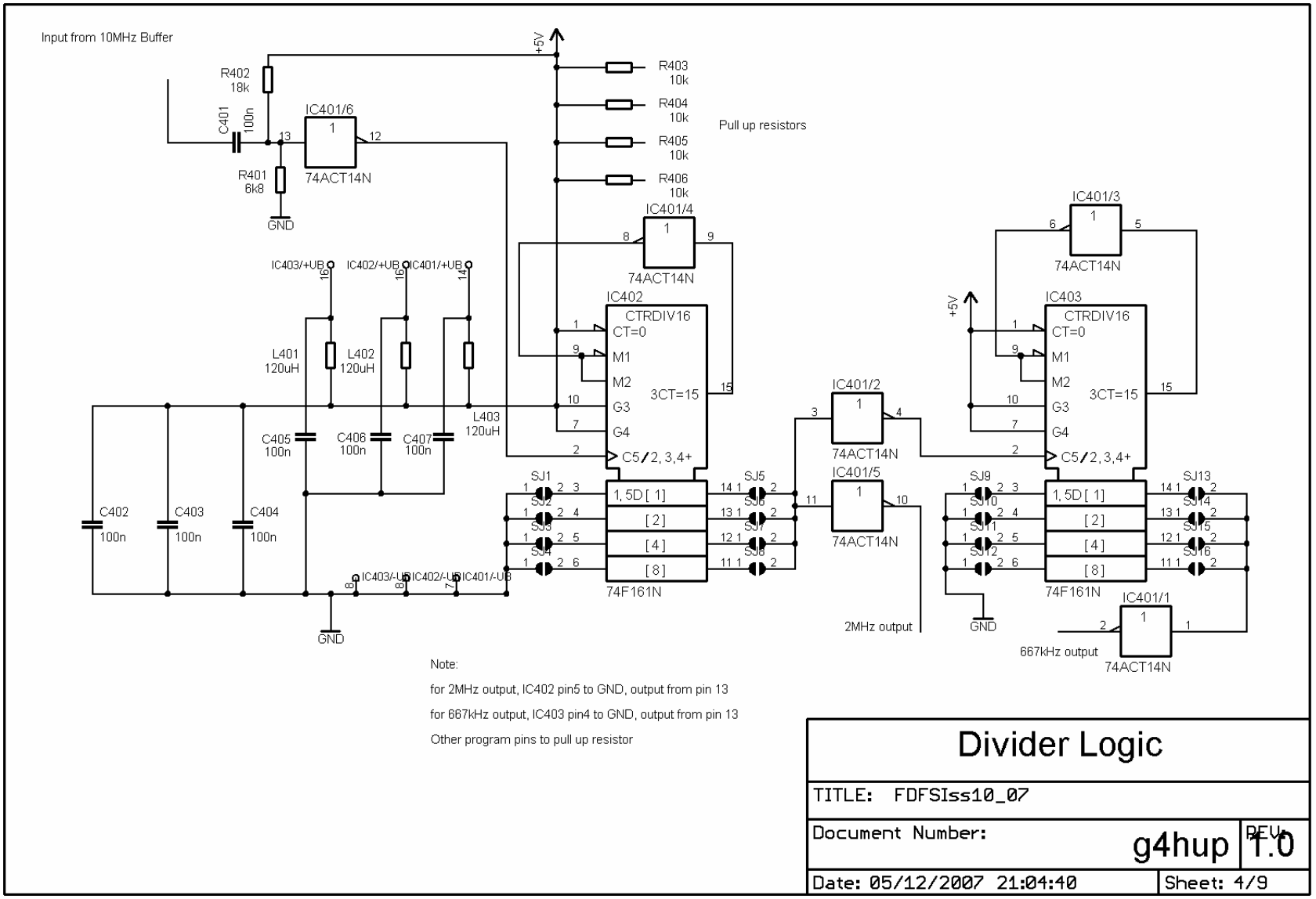

Fig 4 – Logic Stages Circuit Schematic

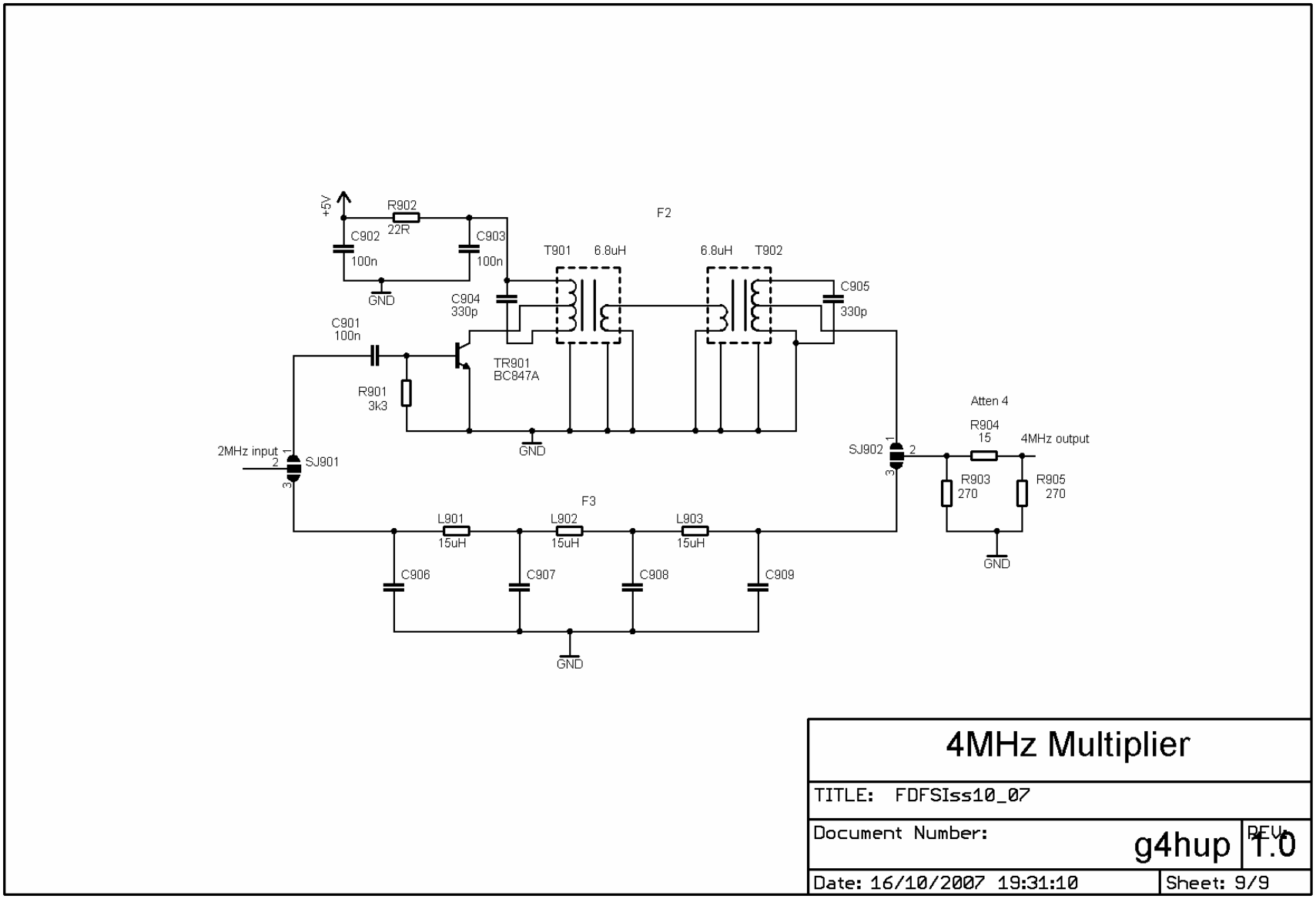

Fig 5 – MF Amplifier and Multiplier Circuit Schematic

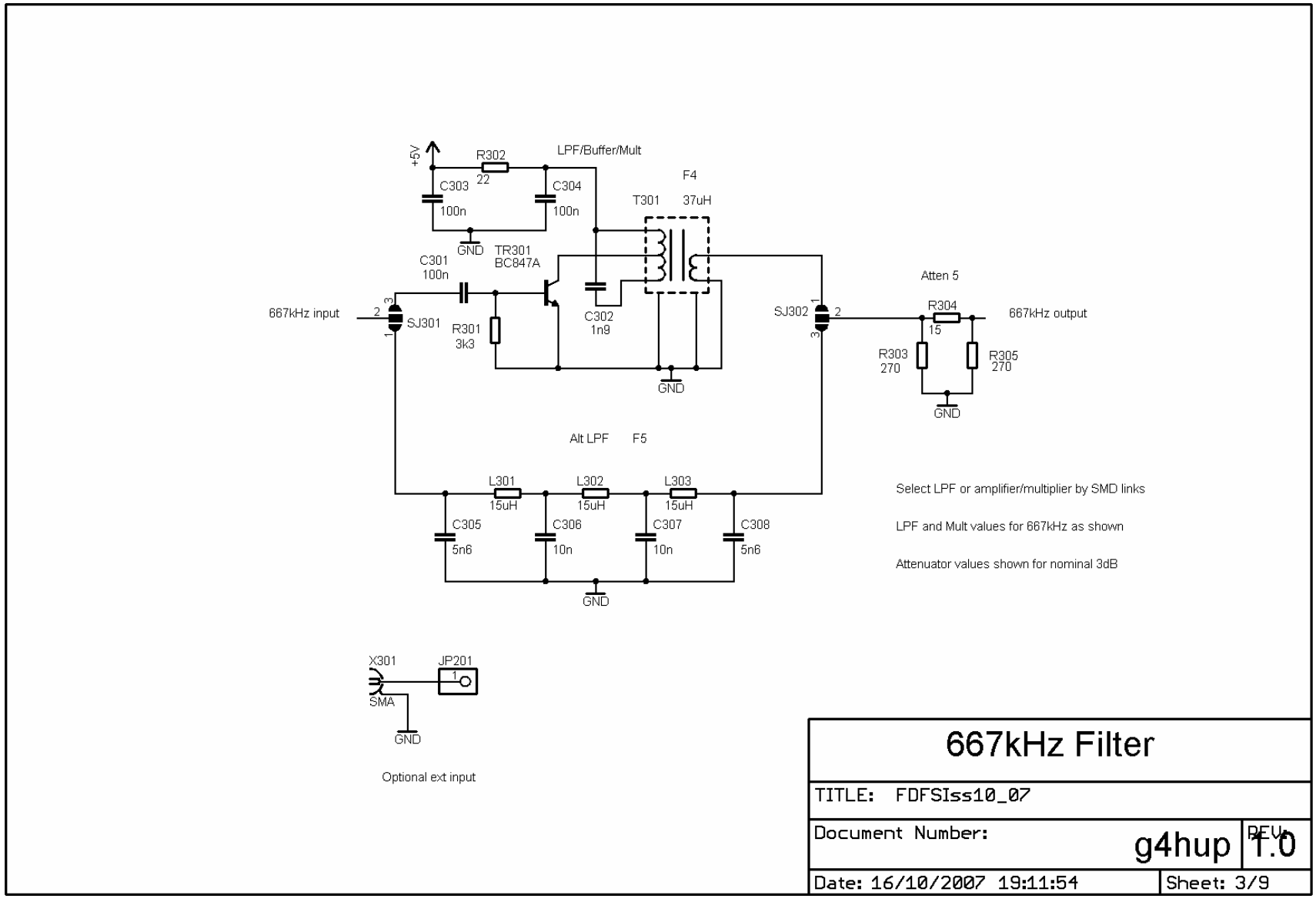

Fig 6 – LF Low Pass Filter / Multiplier Circuit Schematic

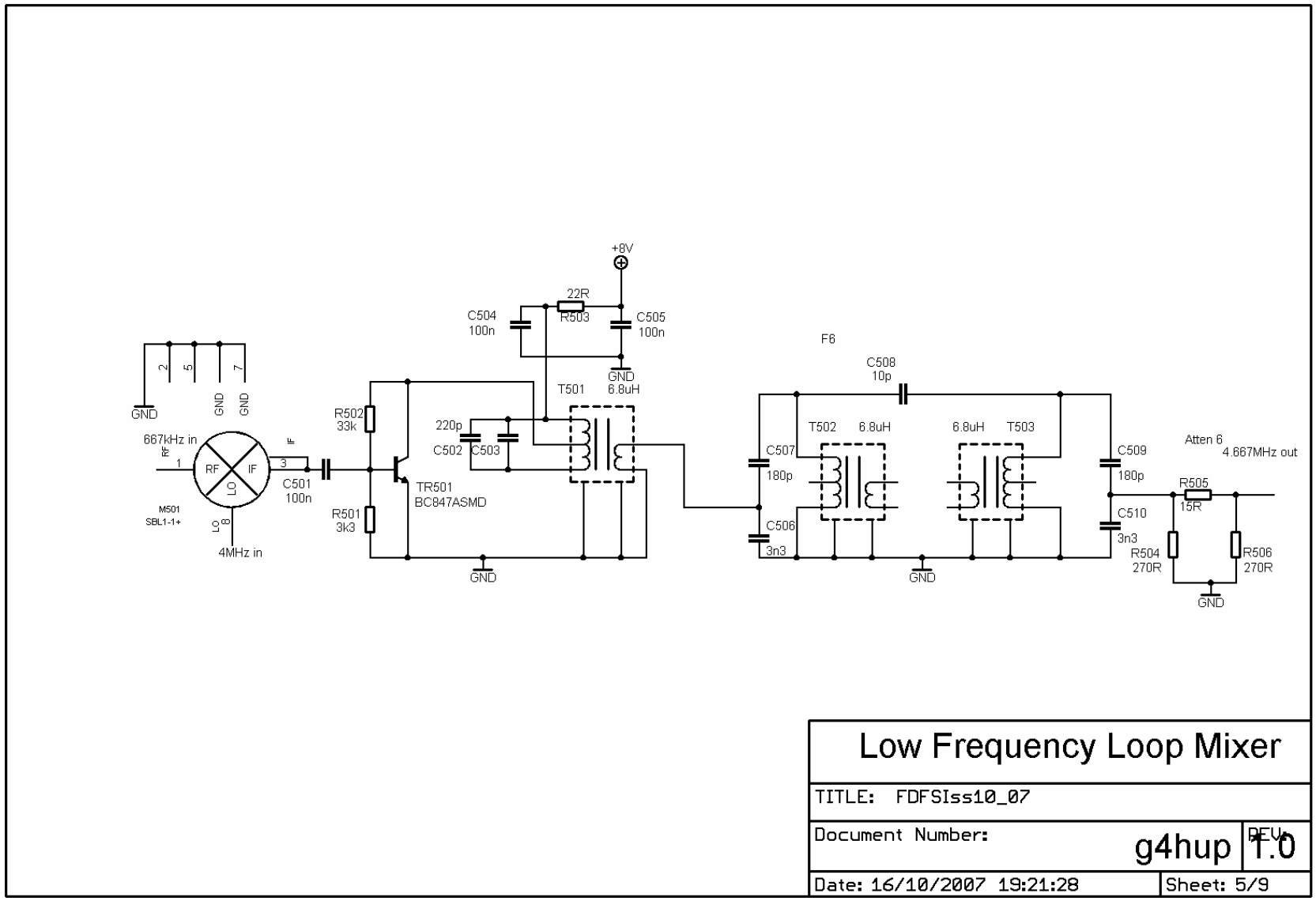

Fig 7 – Low Frequency Loop Mixer Circuit Schematic

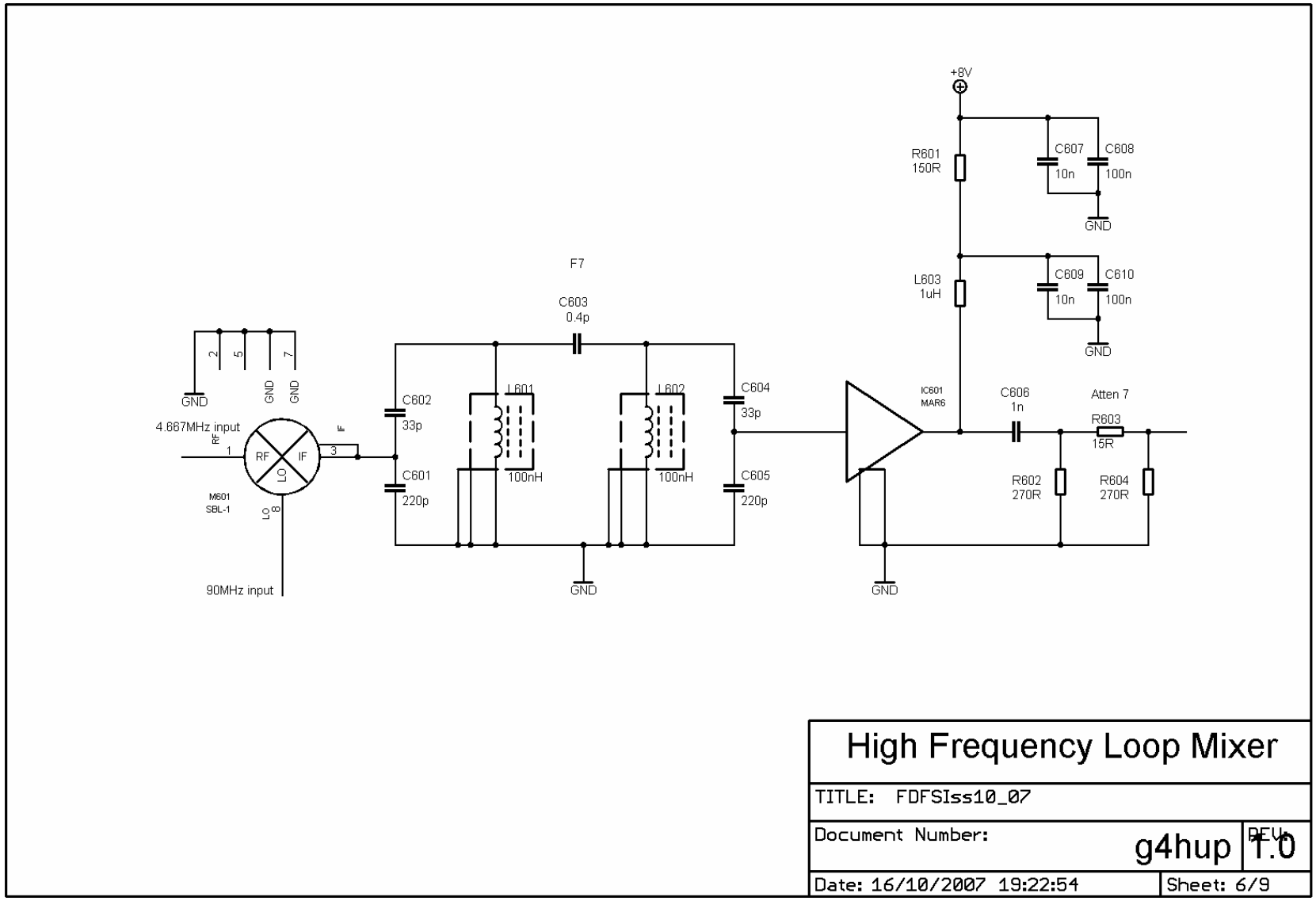

Fig 8 – High Frequency Loop Mixer Circuit Schematic

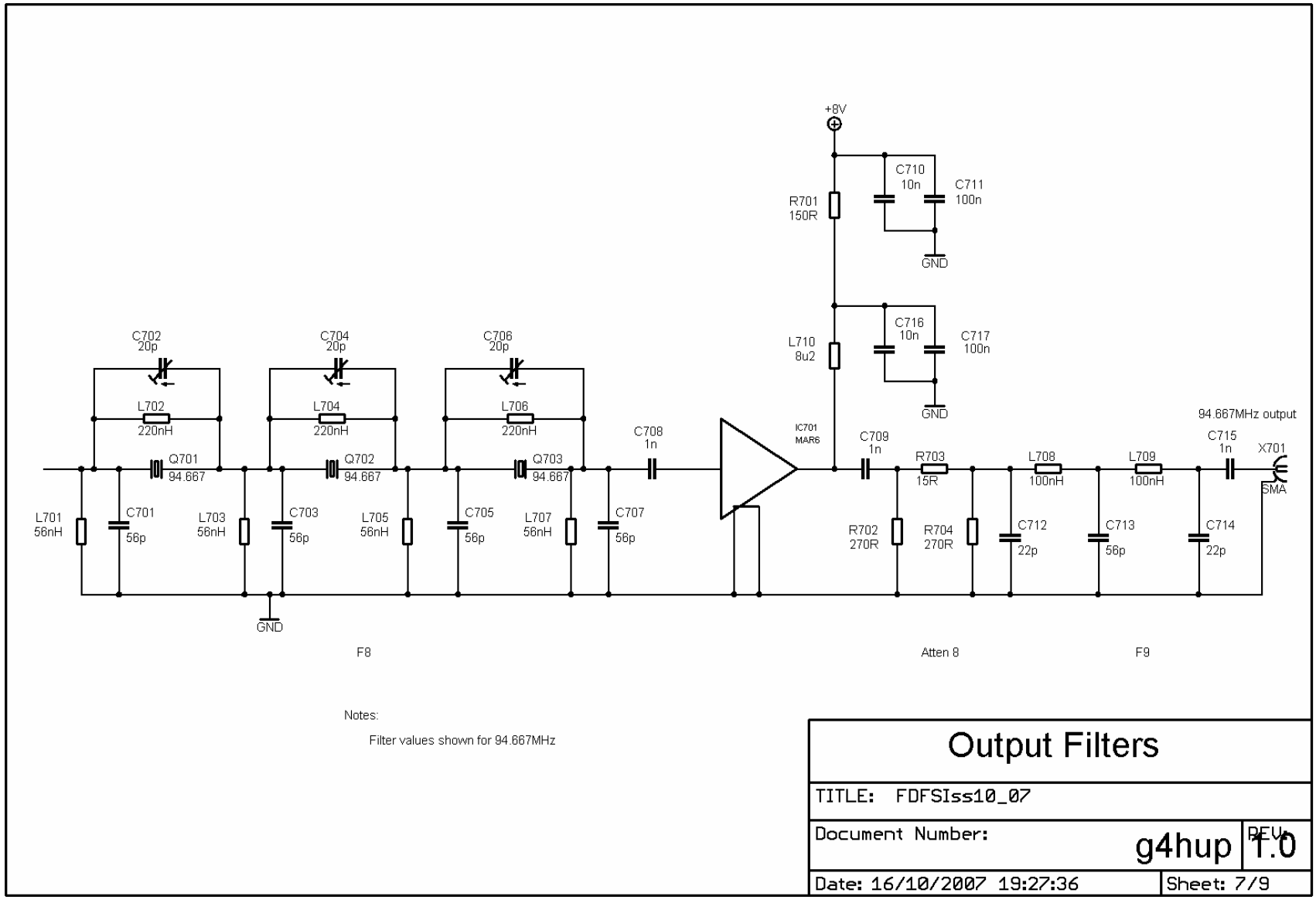

Fig 9 – Crystal Filter and Output Amplifier Circuit Schematic

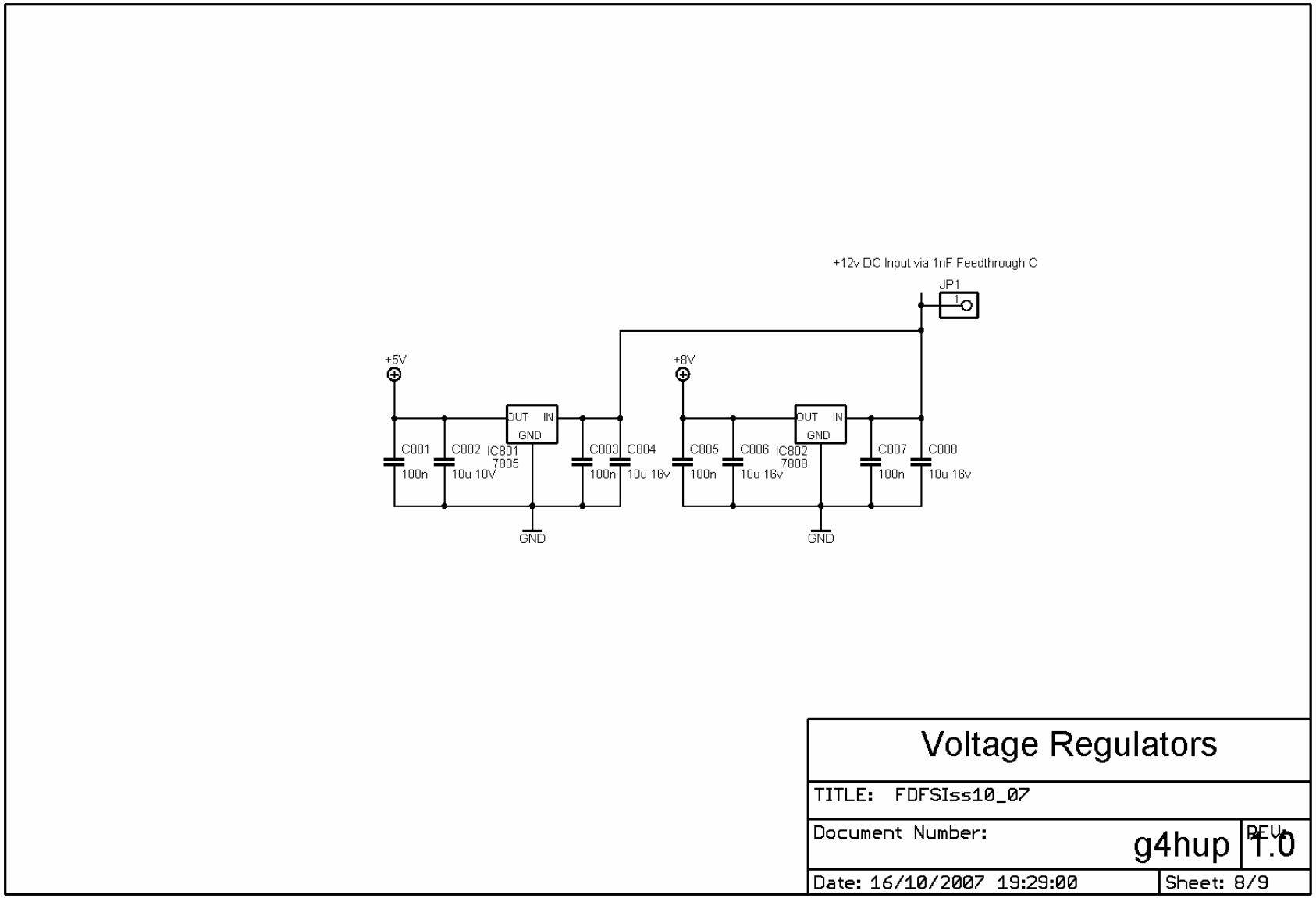

Fig 10 – Voltage Regulator Circuit Schematic

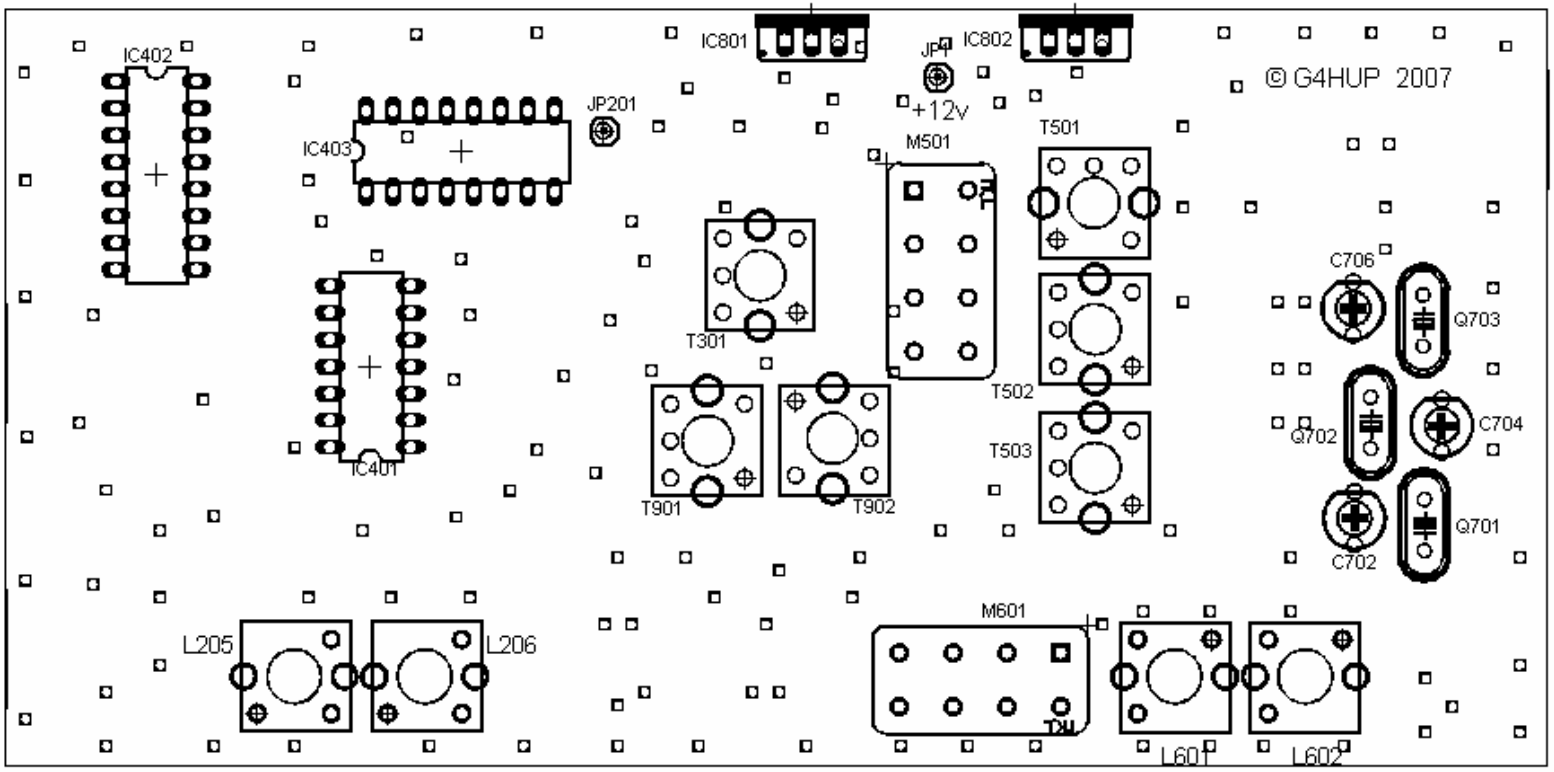

Fig 11 – Top Side PCB Component Locations

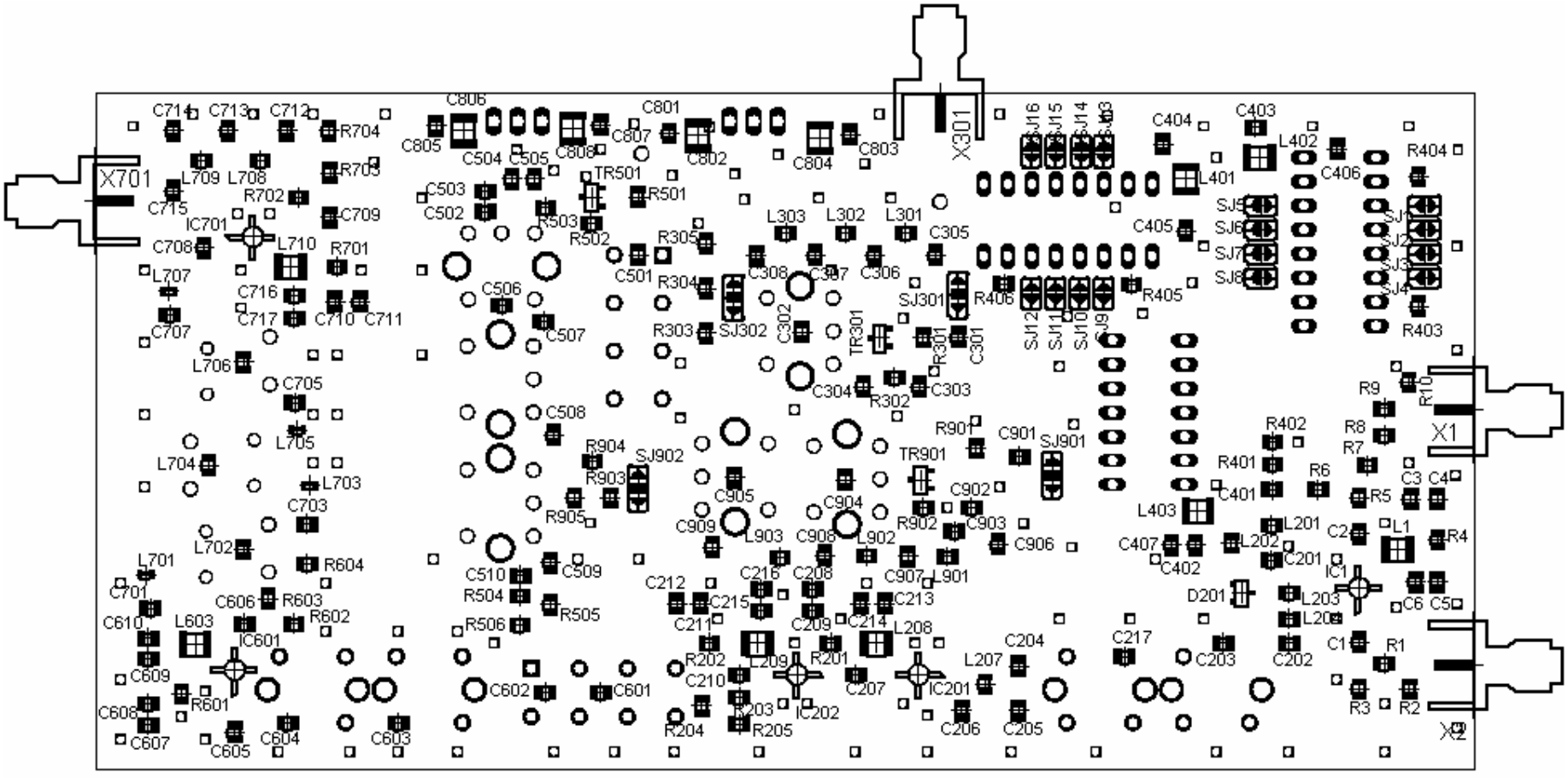

Fig 12 – Bottom Side Component Locations