G4HUP

# Direct Frequency Synthesiser

# Technical Manual – Issue 3

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# Contents

## Unit Specifications

Model Ref

Serial No

| | | |
|---|---|---|
| Input Frequency | 10 | MHz |
| Input Level | +10 | dBm |
| Output Frequency | | MHz |
| Output Level | >0 | dBm nominal - frequency dependent |
| HF Multiplier | | |
| MF Divider Ratio | | |
| MF Multiplier | | |
| LF Divider Ratio | | |
| LF Multiplier | - | |
| Supply Voltage | 10 – 15 | V |
| Supply Current | | mA @ 13vdc |
| Spurii | <-60 | dBc - typical |
| Harmonic output | <-45 | dBc – second harmonic - typical |

## Scope of Document

This document is intended to provide all necessary information to guide users in the installation and configuration of the G4HUP Flexible DFS in normal operation.

Ready built units are supplied to agreed customer specification, and should require no configuration for initial use.

This document is relevant for DFS units constructed on Iss 3_0 PCB's.

Note that for the purposes of information, the circuits in this document are based on the example of a 106.5MHz synthesizer, since this exercises most of the circuit functions. The specific blocks implemented for an individual design will be selected according to the frequency schema required, and as such attenuators and filter designs must be adjusted to suit. Reference data can be found on the DFS web-site, which contains details of all reported implementations – http://g4hup.com/DFS.html . The site also contains typical frequency schemas for popular transverter LO's.

Frequency multiplies used in this manual are based on the assumption of a 10MHz input reference frequency. These must be adjusted if alternative frequencies are used – eg 15MHz.

## DFS Description

The DFS is constructed in a tin-plate housing, measuring 148 x 74 x 30 mm (5.75 x 2.8 x 1.2 inches approx)

External connections are provided for:

- Reference signal in
- Output signal
- +Vcc power supply
- 0v DC ground

All RF connections use SMA female panel connectors

DC connections are by solder terminations to the DC input feedthrough capacitor and the ground tag close by it.

The main circuit blocks are shown in Fig 1, and are described in the following sections, which refer to the circuit diagrams at the end of this manual.

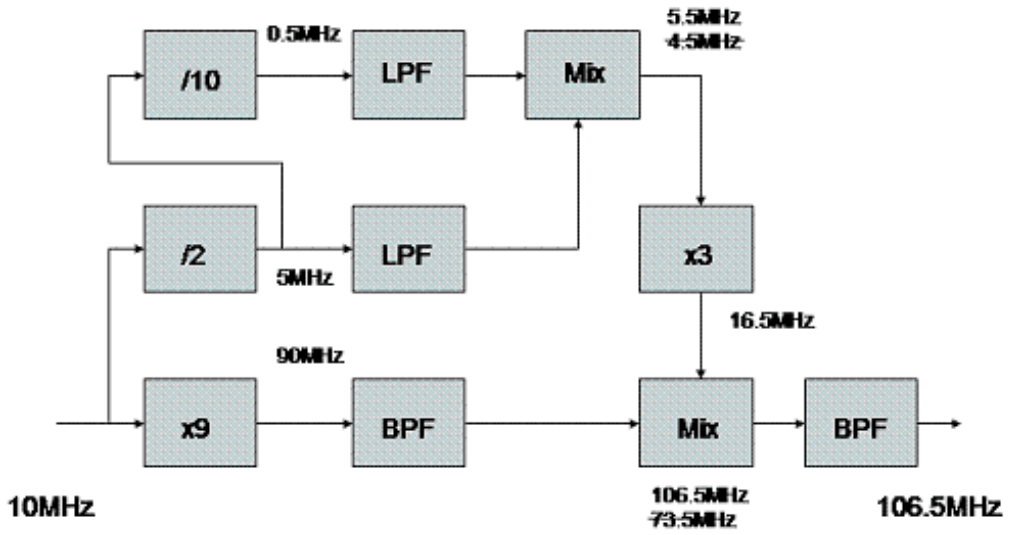



**Fig 1 – DFS block functions – Issue 3**
NB – frequencies quoted are for indication only

### Input Buffer Circuit – Fig 3

NB – this circuit block is not shown in Fig 1 for clarity

The input buffer circuit comprises of an attenuator, MMIC buffer amplifier, resistive splitter and a second attenuator. It needs to be provided where the available input level is less than +10dBm.

The input attenuator values will depend on the available drive level – suitable resistor sets are available on request.

When a drive source of +10dBm or greater is available, this stage can be omitted. In this case strap the input connector directly through to the point where the diode multiplier and the coupling into the logic dividers connect together (junction of C401, L201 and L202). The input attenuator stage, Atten 1, can be implemented if the drive level is significantly above +10dBm.

### Diode Multiplier – Fig 4

The diode multiplier is a comb generator, and produces output components beyond 400MHz. The filter that follows selects the 90MHz (or 110/130MHz) component and reduces the levels of the others to approx -30dBc levels.

This filter, F1, is a two stage LC filter, using capacitive taps at the input and output to match into the surrounding stages. A small top coupling capacitor is used, and it is strongly recommended that the stage is fully screened, with an interstage screen, if the

Toko S18 or similar coils are used. Use of Toko MC120 series coils removes this need, but does result in a slightly higher through loss for the filter (5dB vs 3dB). MC120 coils are supplied as standard.

Two stages of MMIC amplifier are use to bring the output signal to a suitable level (approx +2dBm) to drive the double balanced mixer that follows. Atten 3 can be used to adjust the drive level into the mixer. If it is not required then R204 should be replaced with a short circuit, and R203 and 205 omitted. This principle applies to all other attenuators in the circuit.

## Logic Stage – Fig 5

The logic stages use 74ACT series logic – to ensure optimum performance – these devices are capable of counting to frequencies in excess of 120MHz.

Two dividers and inverter sets are provided, although not all of the inverter gates are used – there are some available for experimentation with other configurations if needed. The arrangement of the dividers allows them to be configured for synchronous counting if applicable, to reduce counter generated noise as far as possible. This is via SMD solder jumpers SJ17 and SJ18. See the paragraphs below for configuration outline – but for any specific version detail, look at the versions and guidance available on the website.

The main input signal to the dividers is taken from the Input Buffer via C401. IC401/6 buffers the signal and produces a logic level square wave – the input to this gate is biased by R401 and R402 to make sure the input signal is in the correct range for a good switching action.

Both divider IC's have programmable inputs using SMD solder links SJ-14 and SJ9-12. the 'wanted' combination of program inputs should be solder linked across to ground, and any remaining open inputs connected to the pull-up resistors R403 – R406. This reduces noise on the unused inputs, and improves the jitter performance of the logic stages.

A Programming Guide is available on the DFS website – go to http://g4hup.com/DFS/Divider Programming_v1.pdf. The guide details the connections that need to be made for each input link of each of the divider IC's. It also has configuration details for SJ17 and SJ18 for cascade (synchronous) counting and independent counting – see sections below.

The output from each divider is also selectable on links SJ5-8 and SJ13-16. For direct outputs, or where an odd harmonic multiplication is to be used, choose the output with the closest to a square wave output – often pin 13. For cases where even harmonic

multiplication is to follow the divider, then selecting an output duty ratio of 80/20 may give better results.

Each IC has optional LC decoupling on the supply to reduce the switching transients that may be fed back to analogue parts of the circuit. If you choose not to use this, replace each L by a short circuit, and omit the capacitor physically furthest away from the power pin of the IC. **Do not** omit all the decoupling!

## Synchronous Counting

Where the two dividers are in sequence, then synchronous counting can be used – in this case the input signal clock to the first divider is also used to control the transitions of the second divider – this is an effective technique for reducing the supply line noise from the counters. To implement synchronous counting, SJ17 and SJ8 should be configured so that pad 2 (centre) is connected to pad 3, as in Fig 2, below

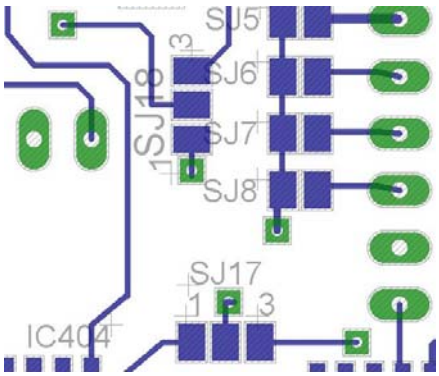



**Fig 2 – PCB detail showing connections of SJ17 and 18**

## Independent Dividers

To use the dividers independently, then SJ17 and SJ18 must be set as pad 1 connected to pad 2. In this case the second signal input is manually strapped via TP1.

## MF Multiplier – Fig 6

The amplifier/multiplier or low pass filter selection is made via SJ901 and SJ902. The two circuits are completely independent, and in some implementations it is advantageous to use both! For example, to generate 4MHz, the multiplier can be used to take the second output of the Input Buffer and double it to 20MHz – this can then be fed into TP1 and divided by 5, which is then passed through the LPF portion of the circuit. The advantage of this is that the lower frequency 2MHz signal is no longer generated – this can help to ease the filtering burden downstream.

A single transistor amplifier stage, TR901, has the tank circuit in the collector tuned to a harmonic – this is capacitively coupled to a second tuned circuit. These two tuned circuits constitute the filter F2.

Alternatively, the LPF, F3, can be used where the output frequency from the divider is the wanted one. It may also be usable for a x2 multiplication (eg where the divider output is 2MHz but 4MHz is required) when the duty cycle of the divider output is 80/20, but this has not been validated. In this case, set the LPF to the wanted frequency, ie 4MHz

Following SJ902 there is an attenuator, Atten 4, to adjust the level into the low frequency mixer – this should be set to around +2 to +4dBm.

## LF Low Pass Filter – Fig 7

As with the MF stage, the LF stage has the option of either amplifier/multiplier, F4, or low pass filter, F5. The appropriate path is selected by SJ301 and SJ302.

Again, there is an attenuator, Atten 5, following SJ302, to set the correct levels for the mixer. Mixer input level should again be set in the +4dBm region

## Low Frequency Mixer and Multiplier – Fig 8

The low frequency mixer combines the MF and LF signals, using an ADE-1 or ADE-6 mixer, depending on the frequencies being handled. Where one of the inputs to this mixer is below 1MHz, then the ADE-6 mixer should be used. This is followed by two stage LC filter (F6) which is capacitively top coupled. The output is tapped down to approx 50R, so the following stages can be omitted if appropriate. Where the amplifier multiplier stage is used, then the combination of C504 and C505 should be replaced with a single capacitor of equivalent value to the two series capacitors. An extra capacitor, marked C504A on the diagram, should be used to directly top couple the output of the filter to the base of the transistor. Some experimentation may be needed to find the optimum value for any particular frequency, but somewhere in the range 10 to 47pF gives good results - see Errata and Addenda section for more information. A single transistor amplifier/multiplier and two poles of filtering follow– the tank circuit of the amplifier stage, is capacitively coupled into another LC tuned circuit, F7. The output of this circuit needs to be at approx 0dBm to get the best performance from the following circuits. Attenuator Atten 6 is used to set this value.

Alternative mixers may be used in this stage according to the frequencies used – check the specification on the Minicircuits website.

## High Frequency Mixer – Fig 9

The second mixer combines the VHF signal from the multiplier chain with the low frequency generated by the loop. It uses an ADE-1 mixer, and is followed by a two stage LC top-coupled filter, F8, to reduce the unwanted components out of the mixer. The LO port input level from the VHF multiplier chain should be set to approx +7dBm (slightly more is OK), and the HF input level should be approx 0dBm – this may not always be achievable. As with Filter F1, MC120 style inductors will be supplied as standard, so there is no need for extra screening.

Alternative mixers be used here – again, check the Minicircuits website for specifications.

The V3.00 PCB incorporates a diplexer following the VHF mixer. This is particularly effective when the LF frequency component is high in value – greater than about 15MHz. For lower LF frequencies, it can be bypassed.

An MAR-6 MMIC amplifier is used to bring up the signal level – this is followed by an attenuator, Atten 7, for gain adjustment

## Crystal Filter and Output Amplifier – Fig 10

A 3 stage crystal filter, F9, using 5$^{th}$ overtone crystals is used to reduce close-in products to the wanted frequency. Careful tuning is required to obtain the best symmetry and balance in the output spurii. DO NOT adjust for maximum output!

Another BGA616 MMIC forms the output amplifier, again with a following attenuator, Atten 8.

The final stage is a low pass filter, F10, to limit the harmonic content present in the output. This provides approx 21dB of suppression at the second harmonic and at least 48dB third harmonic and above.

If you have difficulties getting sufficient harmonic rejection, then it is likely that the levels going into the mixers are too high – increase one or more attenuators by 3dB to resolve this.

## Voltage Regulators – Fig 11

Two 500mA IC voltage regulators provide the 5v and 8v rails – these are mounted on the top-side of the PCB with their associated decoupling capacitors. The DFS unit does run quite warm to the touch – approx 6W is dissipated when running from +13.8V DC. These regulators are used, to save space, and to allow the PCB to be mounted at a height in the box which avoids the SMA sockets fouling the cover lips.

If possible, the DFS should be run from a lower voltage supply – minimum 10v DC. This will decrease the dissipation of the regulators, and allow the unit to run cooler.

Not shown on the diagram is the 1nF feedthrough capacitor, C807, which is used to bring the nominal +12v DC into the circuit enclosure, and the 1N4001 series diode used as reverse polarity protection. The diode should be connected with its cathode (banded end) to the PCB +12v pad and the anode to the FT capacitor.

## Filter and Attenuator Settings

Specific values for filters and attenuators are not given here, since they are very version specific. Refer to the available data on the website for information

See http://g4hup.com for full and latest information on filters and attenuators.

## Errata and Addenda

This section contains information about components that have been changed or added compared with the original PCB design.

See http://g4hup.com/DFSerrata.html for full details, versions impacted and resolution guidance, including pictorial support.

## Component Locations

Figs 12 and 13 respectively show the locations of components on the top side and lower side of the PCB

Fig 14 shows the orientation information for the MMICs and mixers.

## Maintenance

### Construction Practices

In the case of pre-built units, it has been assembled using lead bearing solder - any repairs or changes necessary should be made using lead based solder. Use as small a grade of good quality flux based electronic assembly solder as possible for kit construction.

## *DFS Frequency Schema*

This section provides an area where you can enter the various parameters of your specific DFS version for reference – see completed example in Appendix

| DFS final frequency: | |
|---|---|

| Parameter | Value | | Parameter | Value |
|---|---|---|---|---|
| Input frequency | | | Divider 2 output frequency | |
| VHF Multiplier ratio | | | LF multiplier ratio | |
| VHF frequency | | | LF output frequency | |
| Divider 1 ratio | | | Mixer 1 output | L:<br>U: |
| Divider 1 output frequency | | | IF input frequency | |
| MF multiplier ratio | | | IF Multiplier ratio | |
| MF output frequency | | | IF output frequency | |
| Divider 2 ratio | | | Mixer 2 output | L:<br>U: |

### DFS Filters and Attenuators

In the following tables you can note down the details of each filter and attenuator you require in your DFS – component identities, to match the PCB and schematic legends, and the values of the components.

| Filter | | F1 | | Frequency | | MHz | |
|---|---|---|---|---|---|---|---|
| C202 | | C203 | | C204 | | C205 | |
| C217 | | | | L205 | | L206 | |

| Filter | | F2 | | Frequency | | MHz | |
|---|---|---|---|---|---|---|---|
| C906 | | C907 | | C908 | | C909 | |
| L901 | | L902 | | L903 | | | |

| Filter | | F3 | | Frequency | | MHz | |
|---|---|---|---|---|---|---|---|
| C904 | | C905 | | C910 | | C911 | |
| L904 | | L905 | | L906 | | | |

| Filter | | F4 | | Frequency | | MHz | |
|---|---|---|---|---|---|---|---|
| C305 | | C306 | | C307 | | C308 | |
| L301 | | L302 | | L303 | | | |

| Filter | | F5 | | Frequency | | MHz | |
|---|---|---|---|---|---|---|---|
| C302 | | C309 | | C310 | | C311 | |
| L304 | | L305 | | L306 | | | |

| Filter | | F6 | | Frequency | | MHz | |
|---|---|---|---|---|---|---|---|
| C501 | | C502 | | C503 | | C504 | |
| C504A | | C505 | | L501 | | L502 | |

| Filter | | F7 | | Frequency | | MHz | |
|---|---|---|---|---|---|---|---|
| C506 | | C507 | | C509 | | C510 | |
| C511 | | | | L504 | | L505 | |

| Filter | | F8 | | Frequency | | MHz | |
|---|---|---|---|---|---|---|---|
| C601 | | C602 | | C603 | | C604 | |
| C605 | | | | L205 | | L206 | |

| Filter | | F9 | | Frequency | | MHz | |
|---|---|---|---|---|---|---|---|
| C701 | | C702 | | C703 | | C704 | |
| C705 | | C706 | | C707 | | | |
| L701 | | L702 | | L703 | | L704 | |
| L705 | | L706 | | | | | |

| Filter | | F10 | | Frequency | | MHz | |
|---|---|---|---|---|---|---|---|
| C712 | | C713 | | C714 | | | |
| L708 | | L709 | | | | | |

| Filter | | Diplexer | | Frequency | | MHz | |
|---|---|---|---|---|---|---|---|
| C611 | | C612 | | L604 | | L605 | |

| Attenuator | | 1 | | Value | | dB | |
|---|---|---|---|---|---|---|---|
| R1 | | R2 | | | R3 | | |

| Attenuator | | 2 | | Value | | dB | |
|---|---|---|---|---|---|---|---|
| R202 | | R203 | | | R204 | | |

| Attenuator | | 3 | | Value | | dB | |
|---|---|---|---|---|---|---|---|
| R206 | | R207 | | | R208 | | |

| Attenuator | | 4 | | Value | | dB | |
|---|---|---|---|---|---|---|---|
| R903 | | R904 | | | R905 | | |

| Attenuator | | 5 | | Value | | dB | |
|---|---|---|---|---|---|---|---|
| R303 | | R304 | | | R305 | | |

| Attenuator | | 6 | | Value | | dB | |
|---|---|---|---|---|---|---|---|
| R504 | | R505 | | | R506 | | |

| Attenuator | | 7 | | Value | | dB | |
|---|---|---|---|---|---|---|---|
| R603 | | R604 | | | R605 | | |

| Attenuator | | 8 | | Value | | dB | |
|---|---|---|---|---|---|---|---|
| R702 | | R703 | | | R704 | | |

## *Appendix*

DFS final frequency: 106.5MHz

| Parameter | Value | | Parameter | Value |
|---|---|---|---|---|
| Input frequency | 10MHz | | Divider 2 output frequency | 0.5MHz |
| VHF Multiplier ratio | 9 | | LF multiplier ratio | 1 |
| VHF frequency | 90MHz | | LF output frequency | 0.5MHz |
| Divider 1 ratio | 2 | | Mixer 1 output | L: 4.5MHz<br>U: 5.5MHz |
| Divider 1 output frequency | 5MHz | | IF input frequency | 5.5MHz |
| MF multiplier ratio | 1 | | IF Multiplier ratio | 3 |
| MF output frequency | 5MHz | | IF output frequency | 16.5MHz |
| Divider 2 ratio | 10 | | Mixer 2 output | L: 73.5MHz<br>U:106.5MHz |

### Change History

| Date | Iss No | Comment | Author |
|---|---|---|---|
| 14 May 2008 | 2.0 | First version | G4HUP |
| 13 Dec 2008 | 2.01 | Included reference to programming guide for dividers – added Fig 2, consequential renumbering of subsequent figures. Minor corrections. | G4HUP |
| 15 May 2009 | 2.02 | Modified circuit diagrams to reflect change of F6 coupling, optional MMIC stage before VHF mixer and diplexer following mixer. | G4HUP |
| 8 Nov 2009 | 2.03 | Physical orientation diagrams added for MMICs and mixers | G4HUP |
| 10 Jul 2011 | 3.00 | Updated to V3.00 PCB detail – construction tables and Appendix added | G4HUP |

End of text – Diagrams follow

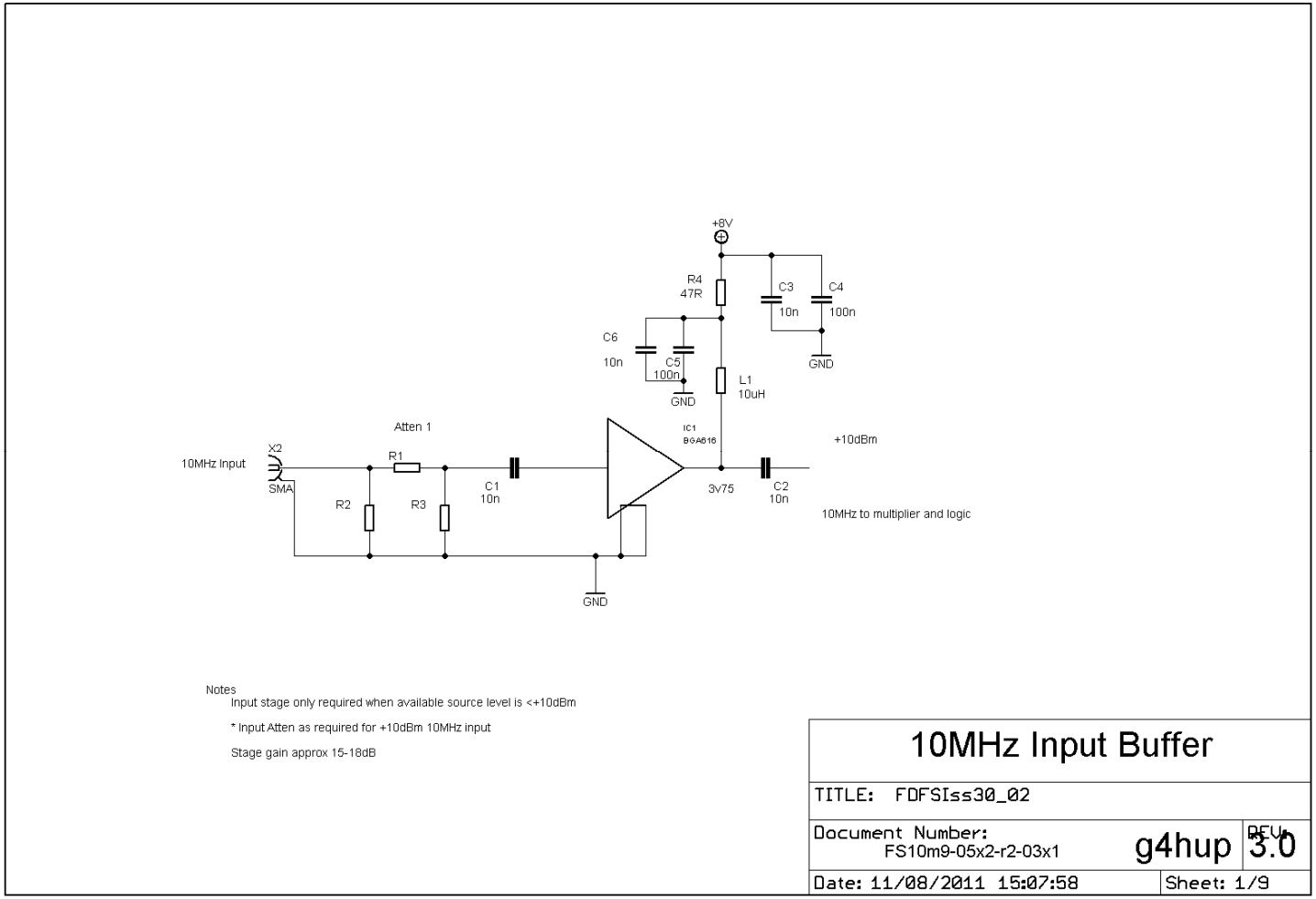



Fig 3 – Input Buffer Circuit Schematic

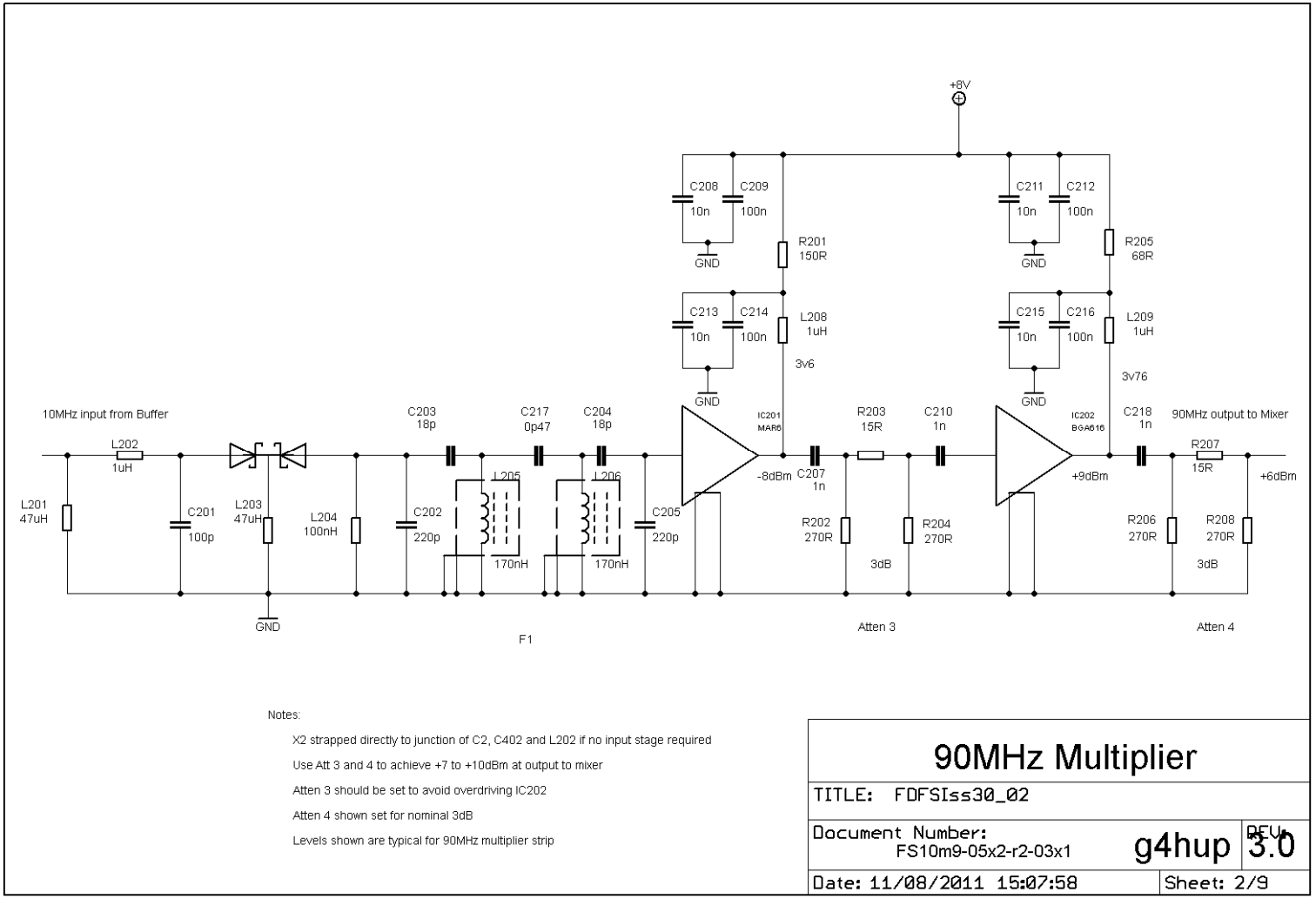



Fig 4 – Diode Multiplier Circuit Schematic

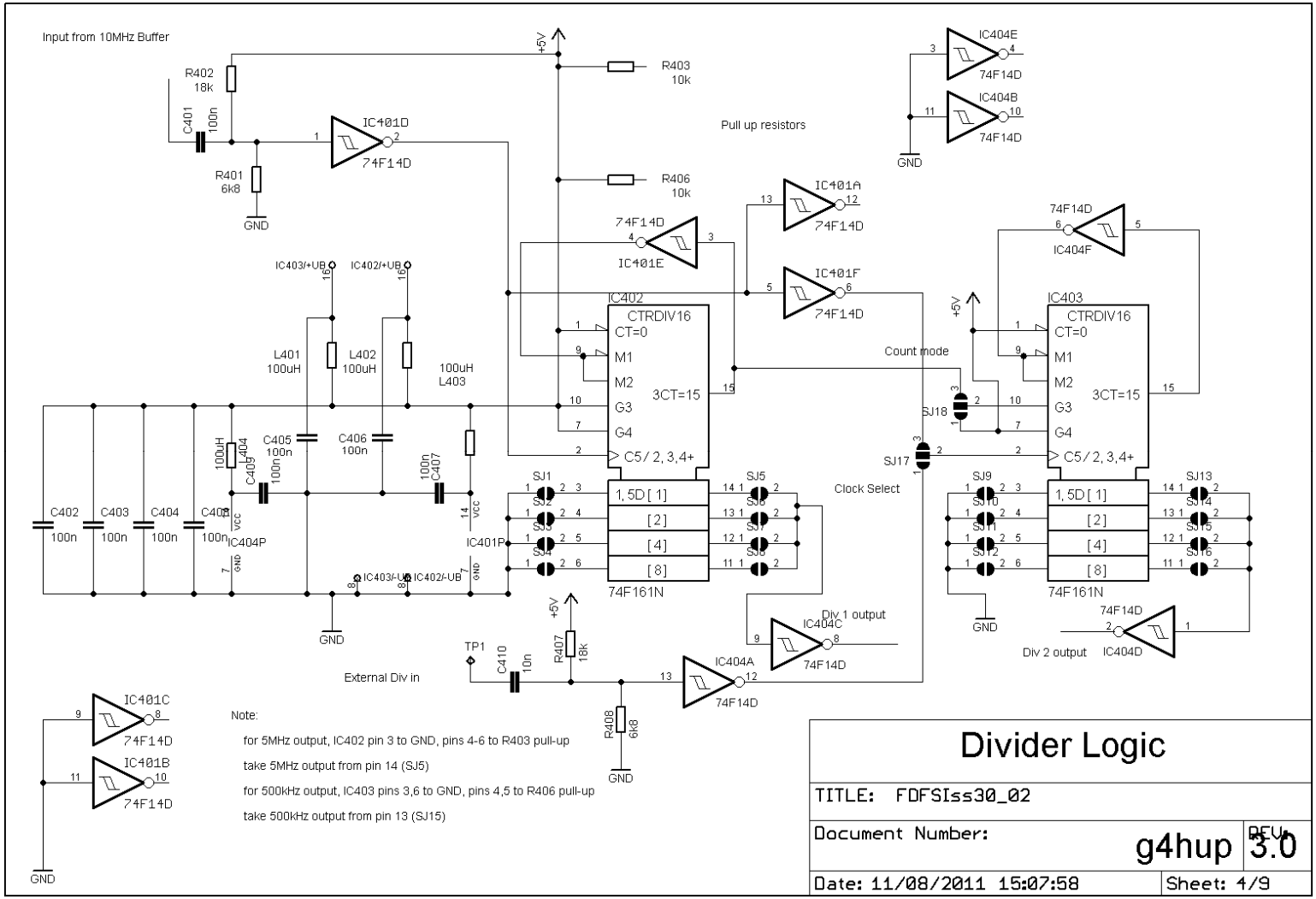



Fig 5 – Logic Stages Circuit Schematic

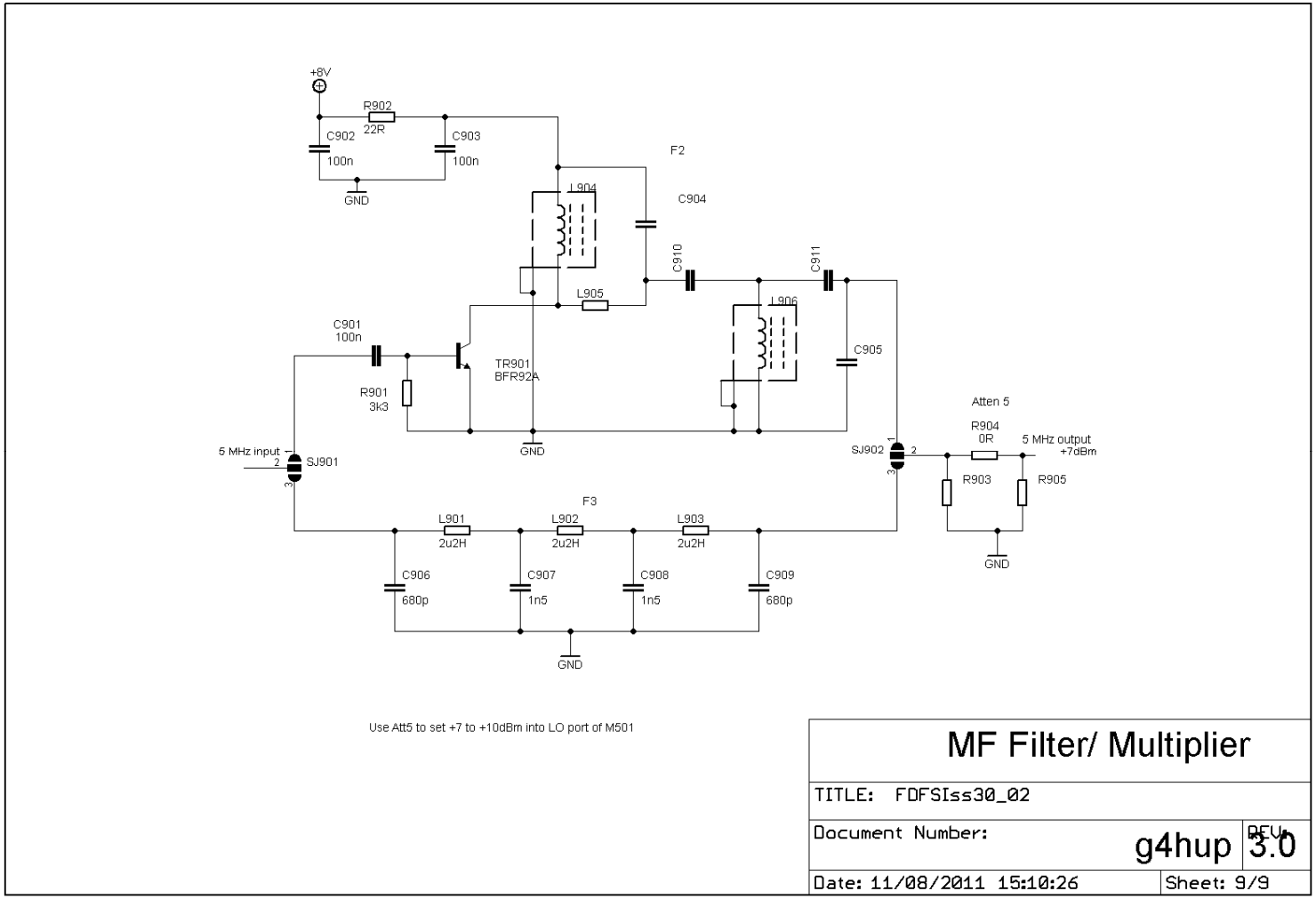



Fig 6 – MF Amplifier and Multiplier Circuit Schematic

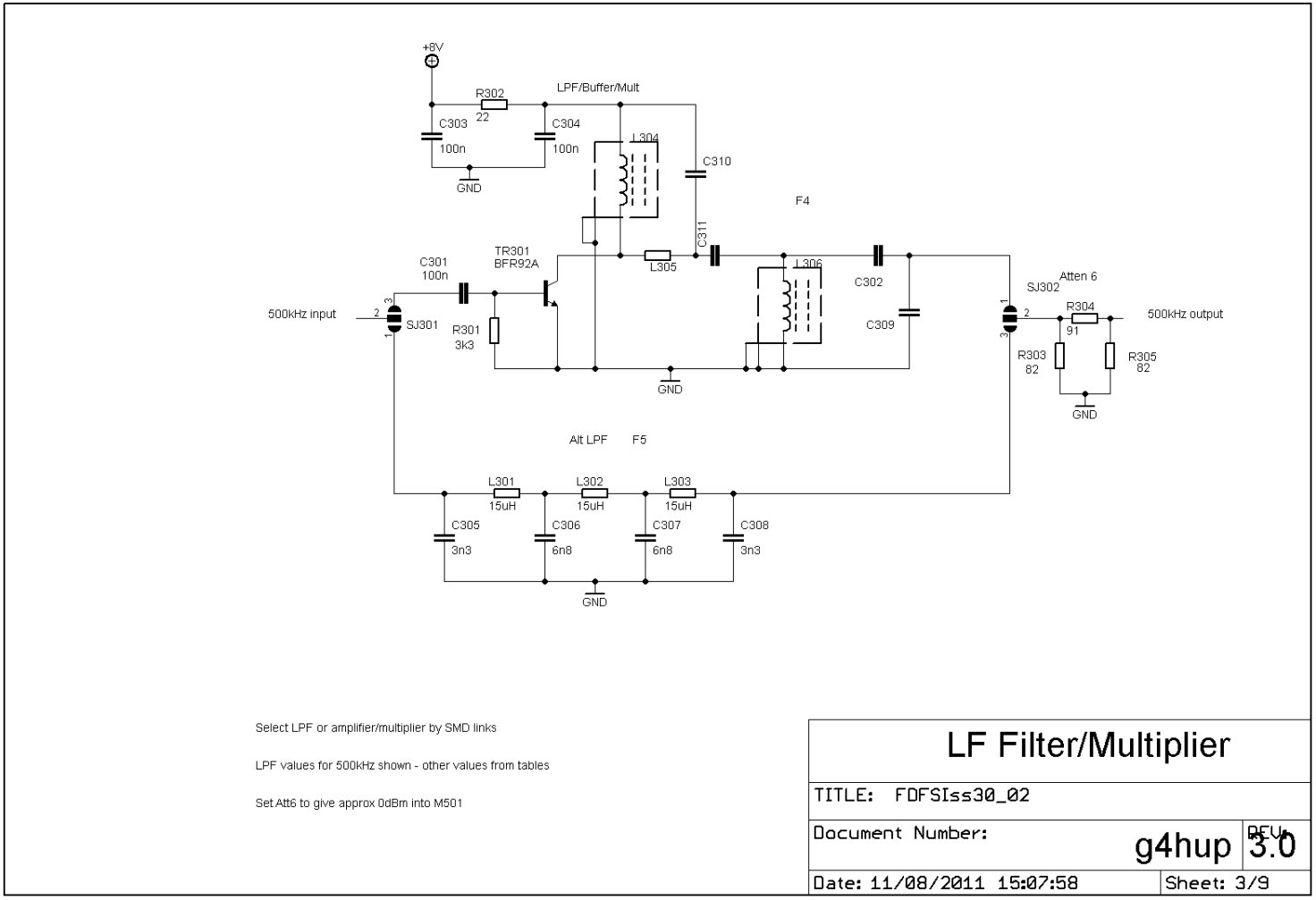



Fig 7 – LF Low Pass Filter / Multiplier Circuit Schematic

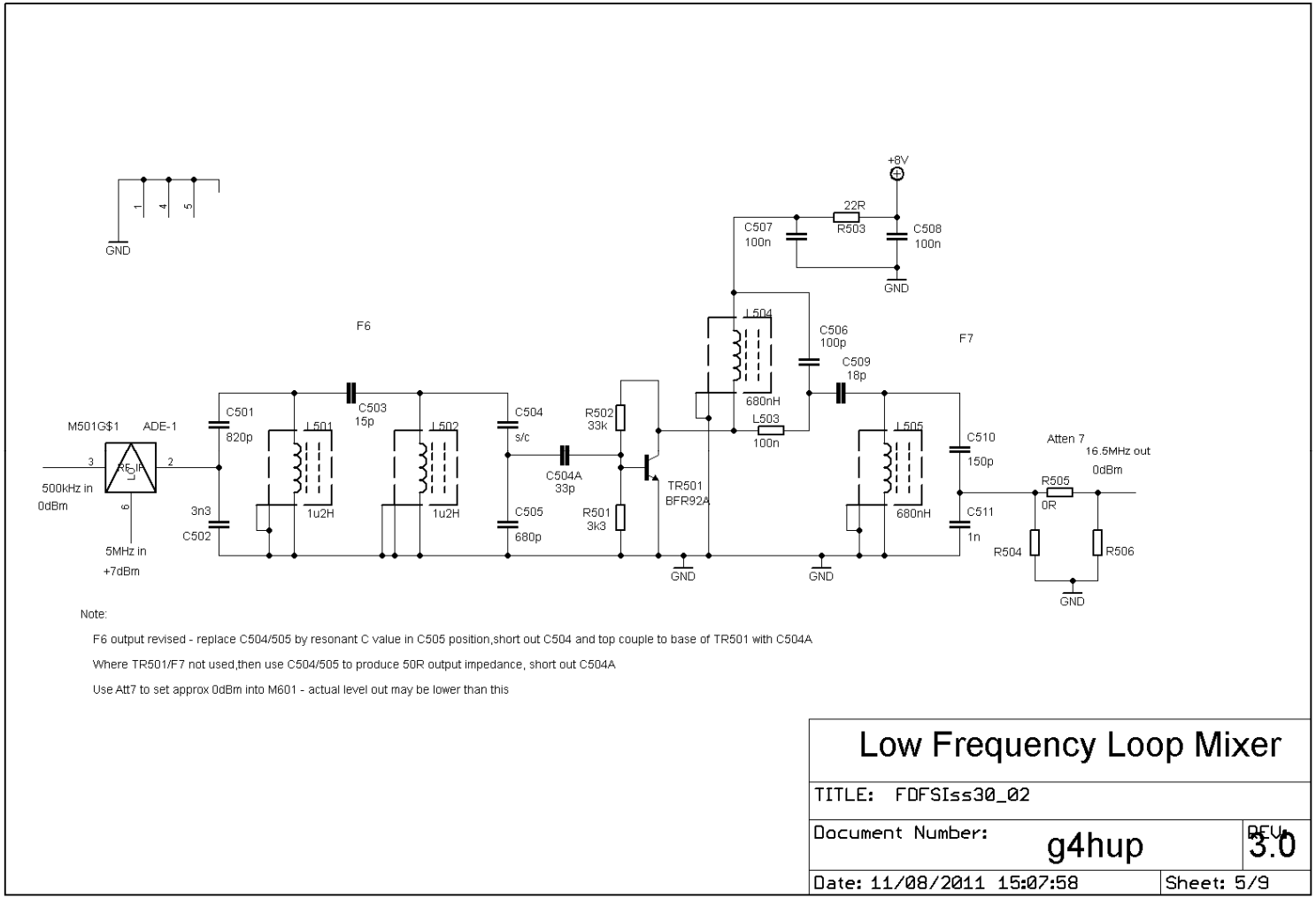



Fig 8 – Low Frequency Loop Mixer Circuit Schematic

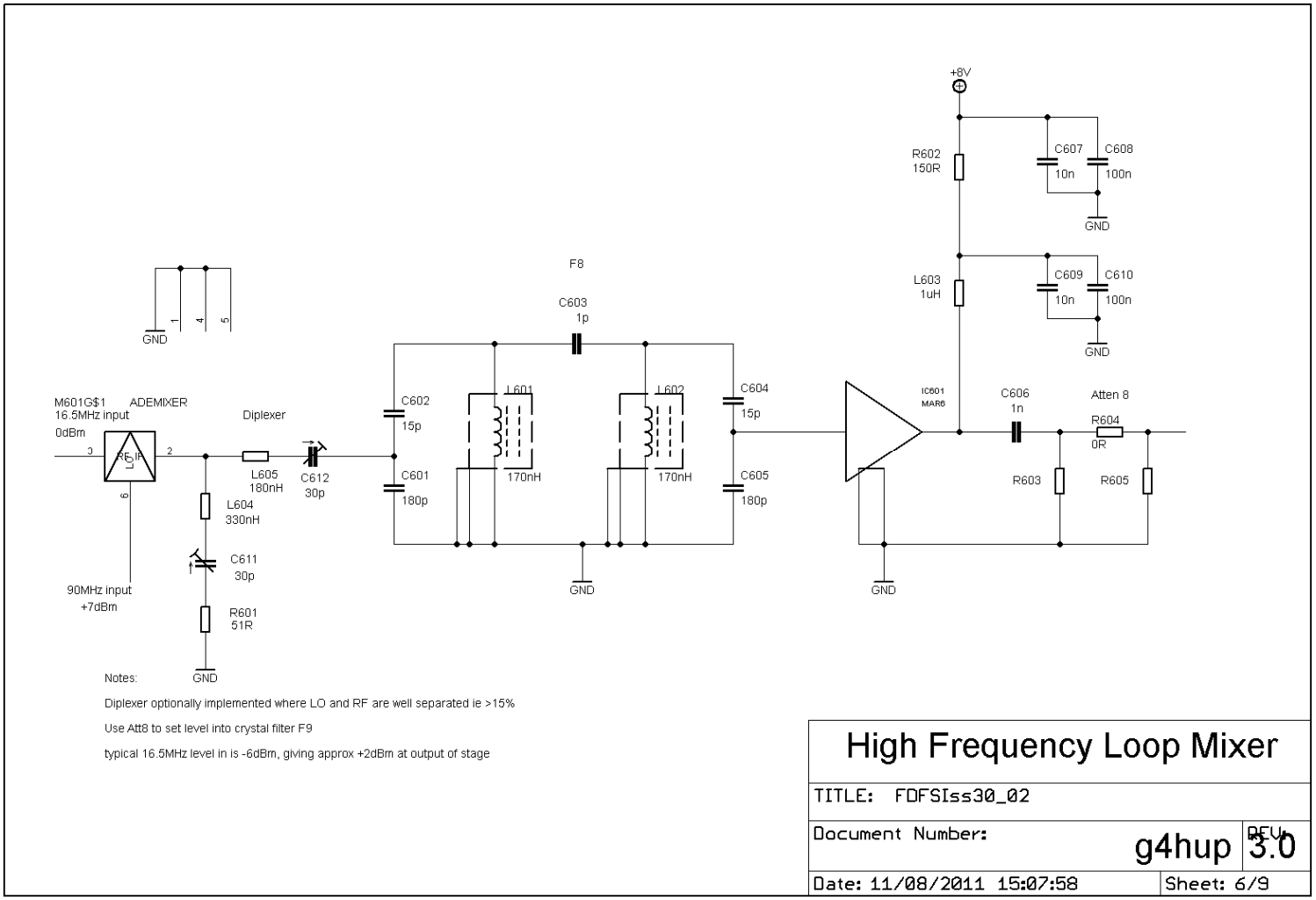



Fig 9 – High Frequency Loop Mixer Circuit Schematic

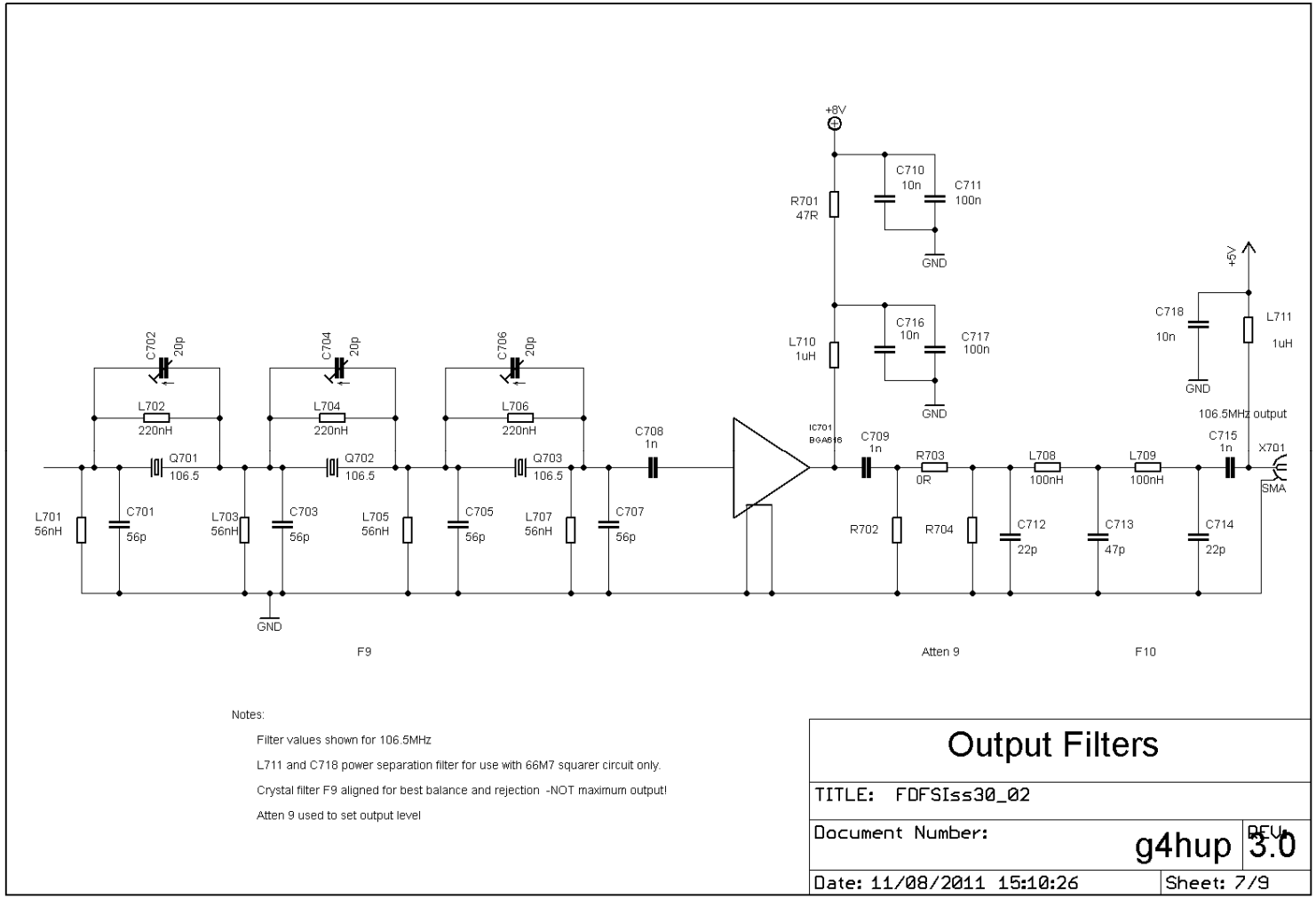



Fig 10 – Crystal Filter and Output Amplifier Circuit Schematic

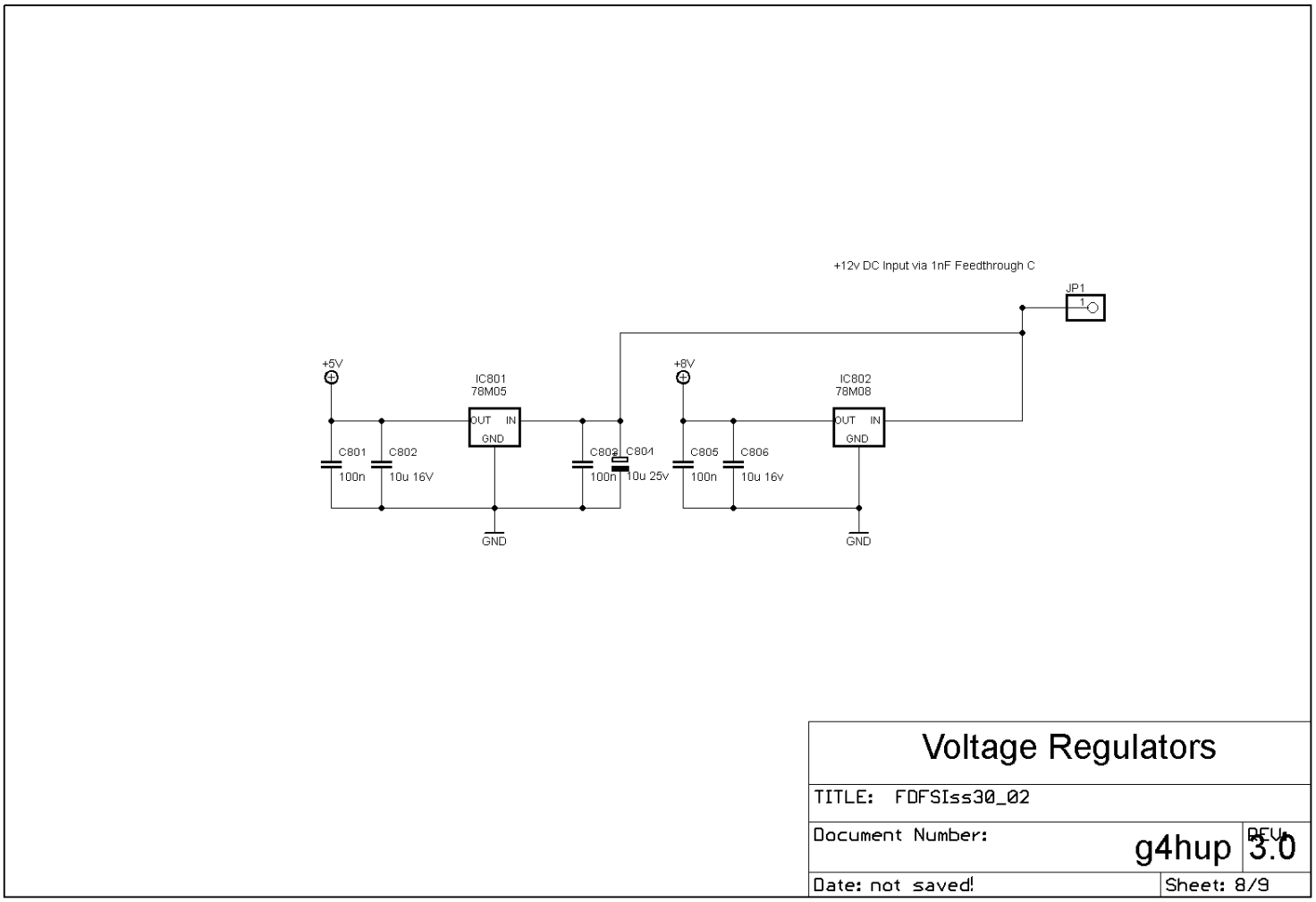



Fig 11 – Voltage Regulator Circuit Schematic

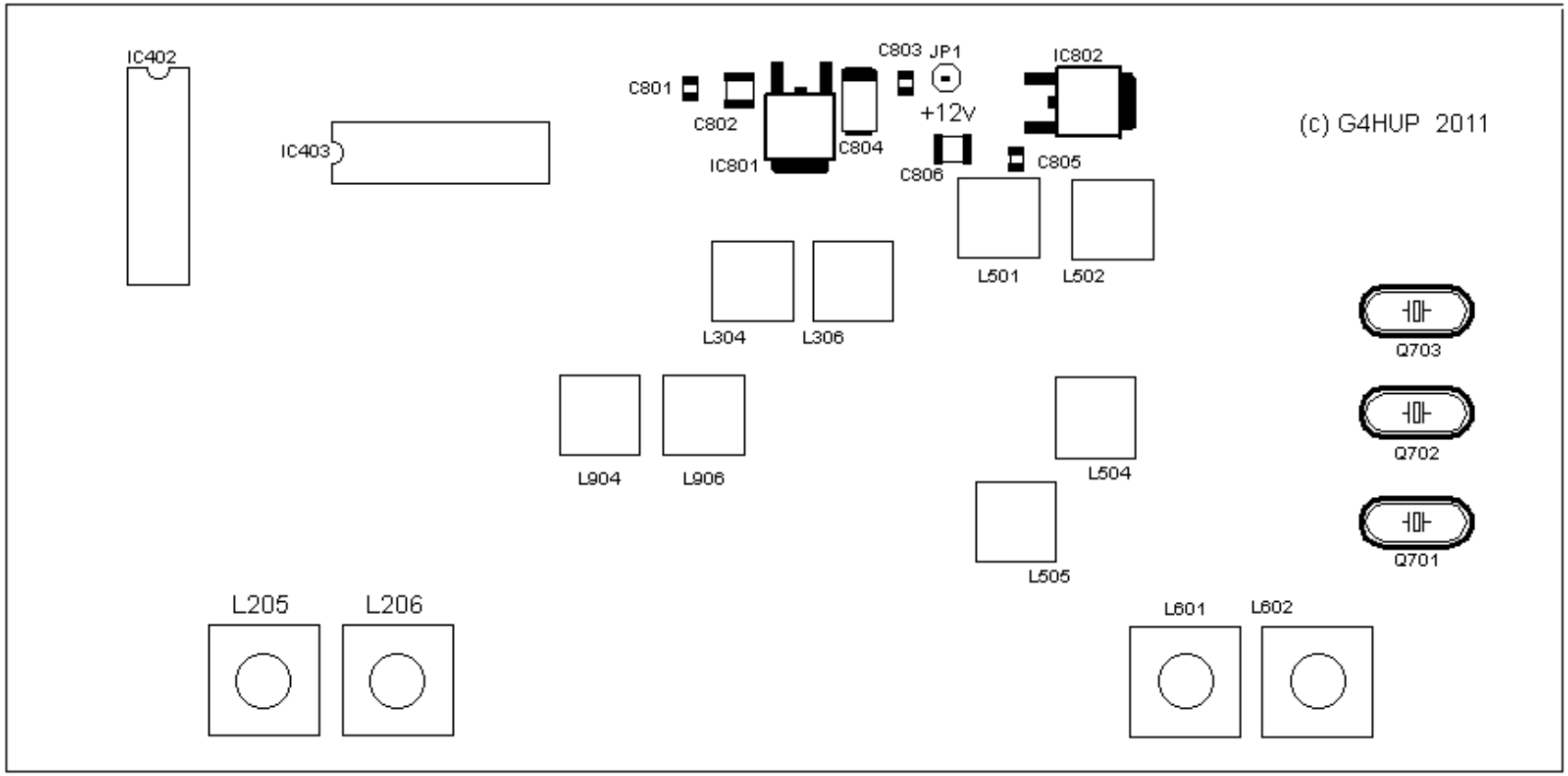



Fig 12 – Top Side PCB Component Locations

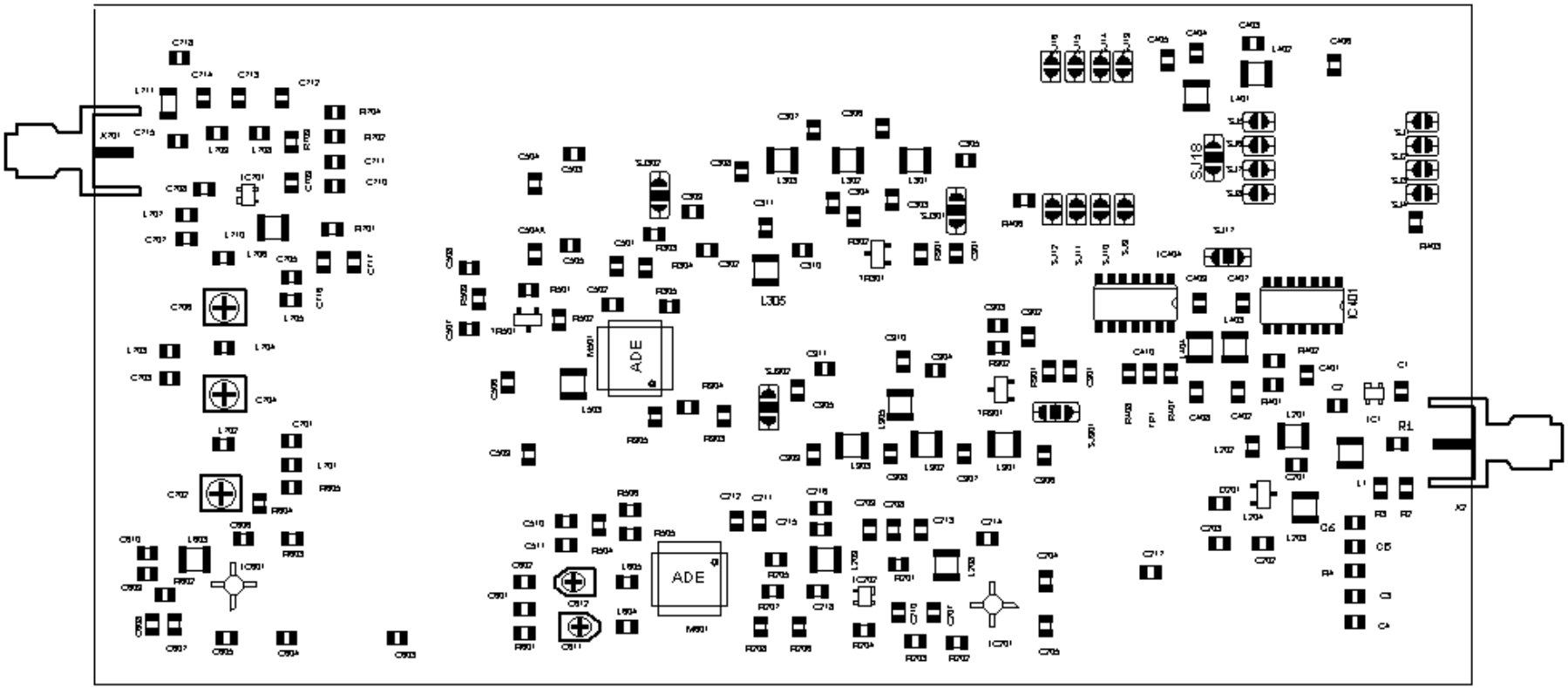
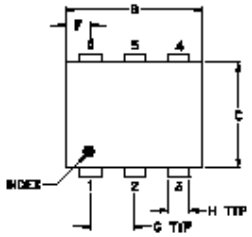
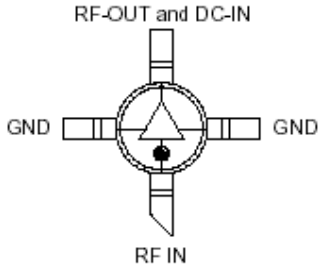



Fig 13 – Bottom Side Component Locations

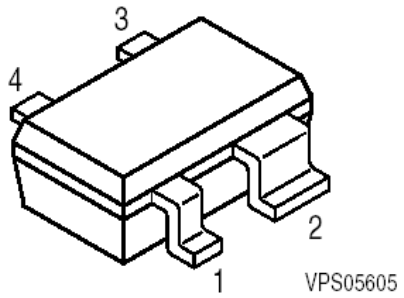



ADE-1 and ADE – 6 mixers




MAR-6

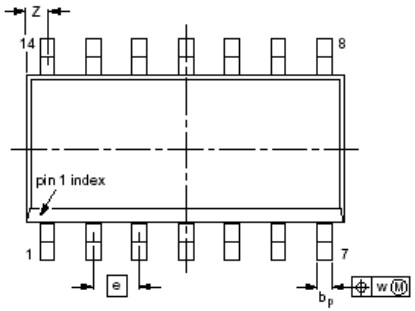
Note – dot on MAR-06 indicates input!!




BGA616

Input – pin 1
Output pin 3
Ground pins 2,4

Pinout data courtesy of Infineon BGA616 data sheet.




74ACT14 SO-14 package

Fig 14 – Component Orientation information