Bias Conditions for MMIC Amplifiers

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Correct bias for microwave transistors is a frequently neglected area. The consequences of inadequate bias conditions range from significantly over-stated specifications, particularly output power capability, to potential failure due to drifts with temperature and power level, and reduced lifetime due to overheating. A discussion and analysis of the problems are presented to assist the engineer when undertaking a MMIC-based design.

pHEMTs present some particular challenges. These devices are still the technology of choice for millimeter-wave applications, in particular for microwave radios at 7 to 40 GHz. Many MMIC circuits require external bias of the gates, with the sources of the transistors internally tied directly to ground to ensure that maximum gain and power-handling capability is obtained. This is particularly true of power amplifiers. The required gate voltage is poorly defined; while generally negative to obtain pinch-off, the value for optimized drain current may be close to zero and of either polarity. In addition to power-on sequencing, most vendors recommend active bias with feedback to the gate voltage to maintain the desired drain voltage and current. However, sometimes these same vendors provide on-wafer test results taken with unregulated bias. This can result in a 2 to 3 dB overstatement of the 1 dB compression point, and inconsistencies in the ratio of output-referred third order intercept point (OIP3) to the 1 dB compression point.

To quantify the importance of this overstatement, we took some measurements with a power amplifier designed for the 13 to 15 GHz band, fabricated by a commercial foundry using state of the art 0.15 micron GaAs pHEMT devices [1]. The amplifier is a single ended three stage design; with paralleled output devices combined using a corporate combiner. This structure is common to many other designs. The amplifier was jointly optimized for third order distortion performance and 1 dB compressed power, as its application was in linear QAM radios with pre-distortion. A ratio of 10 dB between OIP3 and P1dB was achieved in the final amplifier under correct bias conditions. This is significantly greater than obtained in other designs, where the quoted ratio is often in the range 7 to 9 dB. (If the amplifier is modeled as having purely a cubic distortion term, the ratio can be shown to be about 10.5 dB in theory.)

Measurements were taken under two general classes of bias, constant gate voltage (recommended for saturated applications) and constant drain current (preferred for best intermodulation performance when operated below compression). While regulated drain current might seem preferred for all applications, control circuits may be unable to maintain this condition when compression occurs.
Bias Conditions for MMIC Amplifiers (cont.)

Figure 1A shows the measured single tone output power and large signal gain for this amplifier at 15 GHz, with gate bias set to -1.2 V and -1.0 V. It is immediately obvious that the small signal gain differs by less than 1 dB, but the estimated 1 dB compressed output power differs by about 3 dB. The saturated output power is the same in both cases, however the input power for which saturated output power occurs also differs by about 3 dB, with the lower gain and lower (more negative) gate bias case also having lower saturated gain and thus requiring higher input power to saturate.
Bias Conditions for MMIC Amplifiers (cont.)

Figure 1B shows the behaviour of the total drain current for the amplifier. Note that each stage will be at a different level of saturation as the power is increased and this will vary as a function of gate bias. The initial current is lower for the Vgs = -1.2 V case, as expected, but this current begins to increase earlier than the Vgs = -1.0 case, and at saturation the total current is nearly the same for both initial bias conditions.
Bias Conditions for MMIC Amplifiers (cont.)

Figure 1C shows the PAE obtained for the same two cases, showing small variations in PAE at various input power levels, with best PAE depending on the required power level.

Conclusion

Care needs to be taken when interpreting on-wafer test results for commercial power amplifier MMICs. Often the $P_{1\text{dB}}$ is measured at bias levels which are significantly different from the quoted quiescent values. Depending on the actual power levels, OIP3 values may also be established with bias greater than quiescent, although the increase is usually much less than for 1 dB compression measurements. This is due to the lower total output power level generally required for a meaningful intercept point measurement.

For linear applications, active bias is strongly recommended. In non-critical applications, this may comprise a single transistor and a few resistors. In applications where a small sensing voltage drop is desirable, low cost op-amps can be used.

It is highly desirable to ensure that negative gate bias is available before the positive drain voltage is applied to the circuit. This is particularly important to power amplifier designs where the external sensing resistor is kept small to minimize DC power dissipation elsewhere in the radio, and in processes where operation at $I_{\text{dss}}$ may lead to overstressing of devices and shortened lifetime.

References


Bias Conditions for MMIC Amplifiers (cont.)

Appendix

While each application demands a specific approach, three generic circuits are suggested as a starting point for sequencing and bias control.

Sequencer (Fig. 2)

This circuit shows an approach to ensuring that positive drain supply is not applied to the bias circuit until the negative supply is present. A high power FET with low $R_{on}$, is used to give a low voltage drop in normal operation. Resistors R1 and R2 are used to set a threshold at the positive input of comparator. If the “+V IN” is present but the “–V IN” (gate voltage) hasn’t reached its nominal operating point, the level going into the negative supply of the comparator, determined by the input voltages and the R3/R4 combination, will be higher than the threshold and the FET will remain off. Once the gate voltage reaches an acceptable level, the comparator output will go high, turning the FET on, creating a path for the “+V IN” to the drain of the MMIC.

Alternatives include incorporation of the shutdown supply as part of a linear regulator, or incorporation of the power FET as part of a linear regulator. Another option is to limit the short circuit current that may be drawn, possibly with a crowbar style foldback action. This last option requires that each individual circuit be so protected.

Low Tolerance Active Bias (Fig. 3)

A simple active bias supply using a low power PNP transistor, has been successfully used for LNA and buffer amplifiers, where the drop across the sensing resistor $R_s$ is large relative to the temperature compensated error in the $V_{be}$ of the PNP transistor, $Q_1$. Diode $D_1$ partly compensates for the $V_{be}$ change over temperature, which is typically 2 mV per °C for silicon transistors. This circuit is generally adequate if the nominal drop across $R_s$ is around 1 volt. In this circuit, $C_1$ and $C_2$ represent the high frequency bypassing close to the MMIC, typically microwave single layer capacitors of value 100 pF to 2 nF. $R_1$ and $R_2$, in conjunction with $D_1$, set the base voltage of $Q_1$ at a level 0.7 volts below the desired drain voltage for the MMIC. $R_s$ sets the desired emitter current in $Q_1$, and $D_2$ through $D_4$ ensure that the gate of the MMIC never exceeds two diode drops negative or one diode drop positive. The effective transconductance for a single supply, multi-transistor MMIC may be high, typically >0.1 amps per volt, so the low frequency stability of this circuit needs to be analyzed. Additional R-C sections can be included in the gate control line to ensure stability in the kHz to hundreds of MHz range.

Precision Active Bias (Fig. 4)

For power amplifiers drawing close to an amp, it is wasteful to drop a volt across $R_s$. In this case it is worthwhile to put more effort into a precision supply, using a low power low-offset operational amplifier. With millivolt offsets available and op-amps with rail-to-rail capability, the drop across $R_s$ can be reduced to 0.1 volts or less. The penalty in design is ensuring that the transient behavior of the circuit, both under normal power-on and power-off conditions and under fault conditions, is acceptable. Again, with even higher open loop gain than the previous circuit, care needs to be taken to ensure low frequency stability.
Bias Conditions for MMIC Amplifiers (cont.)

Eg. Set \( V_{IN} = 7V \);
\( V^- = 3.5V \)

When \( V_{IN} \) (Gate Supply) = 0V,
\( V^+ = 0.6 * +V_{IN} = 4.2V \)
\( V_g = +ve \)
DRAIN SUPPLY OFF

When \( V_{IN} = -5V \),
\( V^+ = 0.6 * (+V_{IN} - V_{IN}) - 5 
= 2.2V 
V_g = -ve 
DRAIN SUPPLY ON

Fig 2: Generic Sequencer Circuit

Drain Supply

\( V_{IN} \) = 6.5V
\( V_{GS} = 1V \)
Then for \( I_D = 216mA \)
\( R_S = 4.7 \Omega \)

For \( V_D = 5.5V \)
\( V_S = 4.8V \)
\( R_S \times \text{Drain Supply} / (R_1 + R_S) \)
\( \approx 4.8 + 0.7 \)
Let \( R_2 = 1k \), then \( R_1 \approx 180\Omega \)

To set \( I_D \)
- Let \( R_4 = 1k \)
- Increase \( R_4 \) until \( V_D \approx 0.3V \)
- \( R_3 \approx 2.2k \)

Fig 3: Low Tolerance Bias Supply
Bias Conditions for MMIC Amplifiers (cont.)

Eg.
Drain Supply = 5.6V; I_D = 216mA
set V_D = 5.5V,
then, V_RS = 0.1V
R_S = 0.5Ω

At steady state,
V_o ≥ 0V
v+ ≥ v-
so, v- ≥ 5.5V
choose, R_1 = 1k
then, R_2 = 56k

Let, Gate Bias Supply = 5V
and V_S = -0.3V
from before, V_o ≥ 0V
choose R_p = 1k
so, j ≥ 15k

Fig 4: Precision Bias Circuit

About the Authors
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